University of Alberta

Noise and Quadrature Signal Generation Problems in CMOS Radio Frequency Receivers

by

Ahmed Allam ©

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To my beloved parents, brother, and late grandmother.

Abstract

We investigate problems of thermal noise and quadrature signal generation occurring in the design of front-ends of RF CMOS receivers. The performance metrics of quadrature signal oscillators include power consumption, phase noise, and quadrature accuracy. Optimization of quadrature oscillator performance entails a study of CMOS RF noise models and the mechanisms responsible for oscillator phase noise and quadrature accuracy. A major obstacle in CMOS RF IC design is lack of adequate thermal noise models, as existing theories of RF noise in MOS transistors are based on long channel device models. The first goal of our study is an investigation of the noise properties of submicron MOS transistors. The second goal is to provide circuit designers with an understanding of the mechanisms responsible for accurate quadrature signal generation in CMOS LC and RC oscillators.

The first part of the thesis deals with high frequency channel noise measurements and describes designs that were manufactured and measured in the course of thesis development. Several channel thermal noise models suitable for MOSFET devices operating at high frequencies are evaluated. A comparison between extracted and calculated noise data indicates that a recently published simple model of short channel devices operating at RF frequencies provides the best match between extracted and calculated results for channel thermal noise over a frequency range of 3 GHz to 6 GHz and a gate overdrive voltage range of 0.2 V to 1.2 V.

In the second part of the thesis several different implementations of quadrature oscillators are reviewed; also, the design of CMOS RC oscillators is presented. RC oscillators are known to exhibit high phase noise compared to LC oscillators. However, we demonstrate that by increasing coupling in RC oscillators, one can obtain a quadrature oscillator with noise performance and quadrature error comparable to that of an LC coupled oscillator. Measurements were performed on 5 GHz LC and RC quadrature oscillators built in 0.18 μm technology. With increased coupling strength, RC oscillators showed phase noise and quadrature error performance similar to that of LC oscillators.

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List of Acronyms

A/D	analog-to-digital
ASITIC	analysis and simulation of spiral inductors and transformers for integrated circuits
BER	bit error rate
CLM	channel length modulation
CMOS	complementary metal oxide semiconductor
CNR	carrier-to-noise ratio
dB	Decibel
DSP	digital signal processing
DUT	device under test
ESD	electro static discharge
FFT	field effect transistor
FOM	figure of merit
Gnd	Ground
GPS	global positioning system
GSG	ground-signal-ground
GSM	global system for mobile Communications
HBT	heterojunction bipolar transistors
HF	high frequency
HFET	heterostructure field-effect transistors
HP	Hewlett-Packard
IEEE	Institute of Electrical and Computer Engineering
IF	intermediate frequency
IIP_3	third order intercept point
IMD	intermodulation distortion
ISF	impulse sensitivity function
ISS	impedance standard substrate
LDD	lightly doped drain
LDMOS	laterally double-diffused metal-oxide semiconductors

LNA	low noise amplifier
LO	local oscillator
LPF	low pass filter
MIM	metal-insulator-metal
MOS	metal oxide semiconductor
NMOS	N type metal oxide semiconductor
OIP_3	output third order intercept point
$P_{1\text{-dB}}$	1 dB compression point
PA	power amplifier
PCB	printed circuit board
p-HEMT	pseudomorphic high electron mobility transistor
PLL	phase locked loop
PMOS	P-Channel metal oxide semiconductor
RF	radio frequency
RF IC	radio frequency integrated circuit
rms	root mean square value
S parameters	scattering parameters
SAW	surface acoustic wave
SDR	software defined radio
Si	silicon
SiGe	silicon-germanium
SiO2	silicon dioxide
SMA	sub miniature connector type A
SNR	signal to noise ratio
SOLT	short open load thru
ST	schmitt trigger
TSMC	Taiwan Semiconductor Manufacture Corporation
VCO	voltage controlled oscillator
VDP	Van der Pol
VNA	vector network analyzer

WLAN	wireless local area network
Y parameters	admittance parameters
Z parameters	impedance parameters

Chapter 1

Introduction

1.1 Overview

According to Abidi [1], the history of radio frequency (RF) electronics can be divided into two main epochs. The first epoch started with vacuum tubes and lasted from the late 19th century to the 1950s. The worldwide market for receivers for broadcast radio and television drove the demand for RF electronics during this era. In addition, RF and microwave equipment played a major role in military communication during World War II. The first epoch was followed by a period of relative decline when the focus of research communities and the microelectronic industry shifted to microprocessors and digital electronics. During this period, RF electronics was considered a disappearing black art. However, raiding by current researchers and engineers on RF circuit topologies produced during this epoch has partially enabled the excellent performance seen in today's RF products, even compared to the limits of modern microelectronic technologies [2].

Research in the area of radio frequency integrated circuits (RF ICs) was reborn in the late 1980s. Advances in silicon radio frequency bipolar technology enabled the first RF integrated circuit to be constructed at the end of the 1980s [3]. Prior to the appearance of RF ICs, radios were built using printed circuit boards (PCBs) and discrete components. The renewed interest in RF ICs was also motivated by the desire of the worldwide communication industry to spread the use of mobile digital phones [4]. The successful fabrication of RF ICs led to size reduction of digital radios and reduced power consumption, which allowed the increase in stand by and talk times of mobile phones to reach acceptable values. In addition to cellular phones, RF ICs were later used in other "low-gigahertz band applications" such as global positioning systems (GPS), wireless local area networks (WLAN), etc. These highly integrated radio products represented an important new niche for IC manufacturers. Nowadays, the explosive growth in mobile communication and the constant need for more efficient spectral use on the part of service providers has led to the appearance of several generations of mobile communication systems. Each new generation of mobile systems supports higher data rates and operates at higher frequency bands, while the hardware backbone is operated at lower power and wireless products are offered to consumers at reduced cost. New developments in the RF section of a transceiver are constantly needed in order to meet the stringent requirements of the new generation of mobile systems. Several factors contribute to the progressive development of modern wireless transceivers. Innovations in semiconductor device technologies directly affect the cost and performance requirements of modern high-speed transceivers. Other factors are the ability of RF circuit designers to exploit the benefits of a new process and avoid the process limitations, and the ability to design new transceiver architectures aimed at reducing cost and improving performance. This chapter will highlight these factors. First, the benefits and limitations of CMOS technology for RF IC design will be discussed, then modern RF transceiver architectures will be reviewed. Major future trends for the design of RF transceivers will be identified and typical specifications for RF transceivers will be presented.

1.2 Thesis organization

The thesis is organized in 6 chapters. Chapter 1 provides an introduction and an overview of the building blocks of RF transceivers. The architectures of conventional and modern RF front-ends are reviewed. Future trends in transceiver architecture are presented. RF front-end specifications that are related to the current research work are the focus of Chapter 1.

Chapter 2 presents a small-signal model and a noise model used to characterize MOSFETs operating at RF frequencies. State-of-art research topics in MOSFET noise modeling at RF frequencies are addressed. Finally, the components of a tuner based noise parameters measurement set-up are presented.

The steps needed to extract a small-signal MOSFET RF model are explained in Chapter 3. The extraction methodology is applied to MOSFETs with various widths. Comparing the modeled and measured S-parameters validates the extracted small signal model. Steps to extract MOSFET drain current noise are reviewed. A comparison is done between theoretical predictions of several drain current noise models and the measurement results.

In Chapter 4 the main contributions to phase noise theories developed for discrete and integrated devices are presented. LC oscillators are studied in terms of operating frequency, amplitude of oscillations, and phase noise.

In Chapter 5, a structured approach is used to study quadrature signal generation in LC and RC oscillators. First, quadrature LC and RC oscillators are studied using ideal blocks, then the analysis proceeds to circuit level quadrature generation. A synchronization theory for LC oscillators is developed. Simulation and measurement results are used to perform a comparative study of the effects of coupling on RC and LC oscillators.

Chapter 6 summarizes the contribution of the thesis and suggests future research topics.

1.3 The role of CMOS technology in modern RF circuit design

The use of a given semiconductor device technology for the fabrication of RF ICs evolved with time. The chosen semiconductor device technology will depend greatly on the tradeoff between manufacturing cost and RF circuit specifications [5], [6]. Several competing semiconductor device technologies serve as backbones in the making of RF transceivers in current wireless systems. These technologies range from silicon based to compound based devices. Silicon RF CMOS, BiCMOS, silicon germanium (SiGe), heterojunction bipolar transistors (HBTs), and laterally double-diffused metal-oxide semiconductors (LDMOSs) are contending candidates for the RF transceiver blocks from the silicon world. In a III-V compound semiconductor, GaAs-based metal semiconductor field-effect transistors (MESFET's), heterostructure field-effect transistors (HFET's), pseudomorphic high electron mobility transistors (p-HEMT's), and HBTs are commonly discussed technologies for RF circuits. New emerging technologies such as InP based HBTs and p-HEMTs, GaN HFETs, and RF MEMS also show great potential for RF transceiver applications. No single semiconductor technology offers a total solution to integrated RF transceiver building blocks. Different semiconductor device technologies find their own niche applications in certain circuit components but, so far, no device technology provides a universal solution to all circuit blocks in transceiver building modules [5].

Research in CMOS technology for RF IC applications was motivated by the need to integrate the analogue front-end with the digital base band sections. CMOS technology has shown many impressive improvements as a technology of choice for RF applications over the past decade. For example, the scaling of CMOS has increased cutoff frequency (f_t) from 8 GHz at a gate size of 500 nm to greater than 60 GHz at a gate size of 180 nm [5]. Also, CMOS is the technology of choice for low power low voltage circuit design. However, continuous device scaling directly affected CMOS performance as an RF IC technology. While the higher f_t is a benefit, lowering the supply voltage poses a serious problem [1]. First, scaling CMOS devices to lower supply voltages impairs the ability of the RF device to handle signals with a large dynamic range [1]. Another drawback of CMOS scaling is that leakage currents through the source and drain junctions are unavoidable. These drawbacks prohibit CMOS from becoming the technology of choice for wireless front-end circuits for medium to high power (more than 1-W) applications [5]. For these applications, the LDMOS that is compatible with a standard BiCMOS process becomes a more suitable choice. In conclusion, aside from the viewpoint of device technology development, the future of RF CMOS technology will be highly dependent on research and fabrication costs compared to SiGe and III-V technologies that provide superior RF devices and might provide competitive cost structures.

1.4 RF circuit design for modern RF transceivers

An RF transceiver consists of a transmitter and a receiver in a wireless system. Data and voice messages are exchanged through free space [7]. Modern RF receivers are typically composed of two sections: an RF front end and a base band digital section. The RF front end selects an RF modulated signal, amplifies this signal, and down converts it to an appropriate intermediate frequency (IF). The converted IF signal can be demodulated in either the RF section or the base band digital section. Two fundamental receiver architectures are the heterodyne receiver, and the direct conversion receiver. Introducing minor variations to either of the two fundamental receiver architectures can produce other architectures like the zero IF architecture. In each of these architectures, either narrow band low noise amplifiers (LNA) or wideband amplifiers are used as gain stages. Mixers, oscillators, and phase locked loops are used for frequency translation. Integrated filters or bulky off chip filters can be used for RF signal selection.

1.4.1 Superheterodyne receivers

Figure 1 shows a block diagram of a radio receiver built using a superheterodyne architecture [7]. The front-end filter prevents unwanted signals from saturating the low noise amplifier (LNA). Filters decrease receiver sensitivity, thus filtering is often broken into two or more parts to provide sufficient selectivity while minimizing loss of signal. The main function of the low noise amplifier is to provide enough gain to overcome the noise generated by the following stages of the architecture; this will be discussed in section 1.5.1.

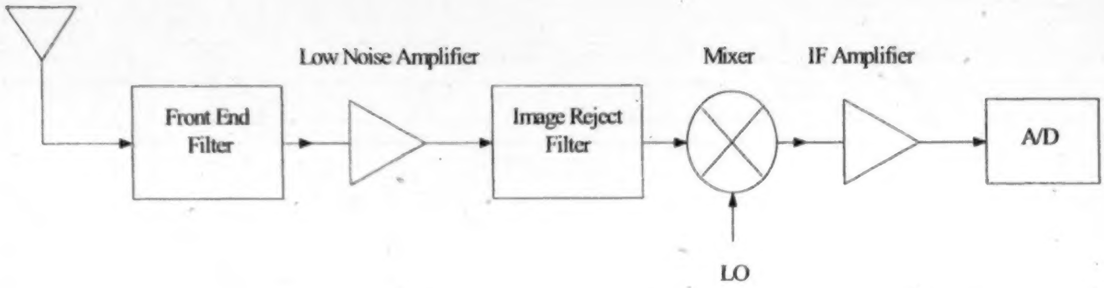


Figure 1-1: Superheterodyne receiver.

The local oscillator (LO) and the mixer convert the RF signal to an intermediate frequency (IF) signal. The output of the mixer is applied to an IF amplifier and filter to obtain a suitable signal for processing by the analog-to-digital (A/D) converter and the demodulator circuits. Advantages offered by the superheterodyne architecture are high selectivity, high linearity, and the possibility to avoid I/Q mismatch [7], [8]. However, requirements of modern receivers highlight several disadvantages in this architecture. One disadvantage is the tradeoff between selectivity and sensitivity caused by the choice of IF frequency (frequency planning). The selection of a high IF frequency leads to high rejection of image frequency (selectivity), but requires a highly selective image-rejects filter causing gain losses in the signal band (sensitivity). Another disadvantage of this stage is its vulnerability to spurious signals such as interference at the half IF frequency [7]. Modern wireless receivers are required to operate with a minimum amount of power consumption. The high number of components involved in superheterodyne architecture makes it difficult to meet this requirement. Another drawback of this architecture is the need for a highly selective off chip surface acoustic wave (SAW) filter. The presence of fixed bandwidth SAW filters disqualify this architecture from use in multimode, multistandard transceivers.

1.4.2 Direct conversion receivers

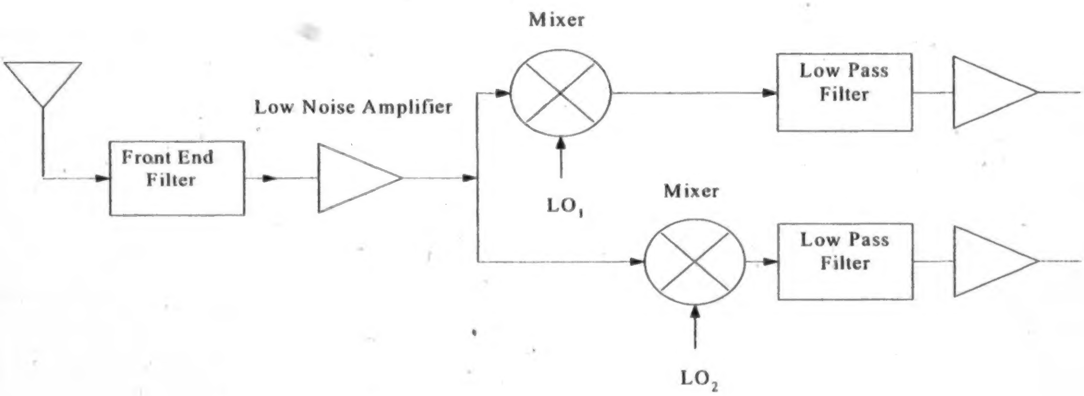


Figure 1-2: Direct conversion receiver.

In direct conversion receivers, the incoming RF signal is directly down converted to zero IF frequency by an oscillator whose frequency is equal to the RF signal. A block diagram of this receiver is shown in Figure 1-2. A single low pass filter filters the converted signal. As the two sidebands of the RF incoming signal contain different phase information, down conversion must provide quadrature outputs in order to avoid loss of information [7]. The direct conversion architecture offers several advantages. First, off chip SAW filters are eliminated and second, power consumption is reduced in this architecture due to the reduction in number of frequency translation components.

Despite the fact that the direct conversion architecture allows for higher levels of integration, it suffers from several drawbacks. The LO signal can leak to the antenna through the finite substrate resistance and the reverse isolation of the elements that precede the antenna. The leaked signal can interfere with other RF receivers operating over the same band. Also, the reflected signal can be mixed with an incoming RF signal and down converted to base band, corrupting the RF signal (self-mixing). As the IF signal is at zero frequency; offset voltages can corrupt the desired signal and saturate the receiver. DC offsets can be caused by self-mixing of flicker noise. Offset cancellation techniques can be used in direct conversion receivers to alleviate the DC offset problem.

1.4.3 Future trends in radio transceiver architectures

Current radio chips are built by integrating the RF section and the digital section on the same die. This integration faces several challenges. Process variations in CMOS technology pose serious limitations to RF IC fabrication. Two solutions have been proposed: radios with auto calibration and control using digital signal processing (DSP) techniques and software defined radios. While, the former solution suggests using DSP techniques to overcome the performance limitations of various radio blocks, the later solution suggests pushing the A/D as close as possible to the receiving antenna.

1.4.3.1 Radios with auto calibration and control

For integrated transceivers, spurious signals and noise generated by the digital section degrade the performance of RF blocks. A solution is needed to enable integrated radios to function in harsh environments and to be less sensitive to process and temperature variations. Built-in auto calibration has been suggested as a solution in [10] to ensure the high performance and robustness of integrated radios. The radios and their integrated blocks are built with adequate calibration and programming capabilities to allow them to adjust for optimum performance. For example, the bandwidth and center frequency of a filter can be calibrated by adjusting the filter time constant. Measuring the in phase (I) and quadrature (Q) channel imbalance and adjusting the phase and amplitude on the I/Q signal can improve the image rejection. A radio with built-in auto calibration and programming capabilities is shown in Figure 1-3. A tiny sensor such as an analog-to-digital converter monitors each of the blocks in Figure 1-3. Each block performance can be measured and evaluated through an algorithm, then tuned to achieve the best performance of the block.

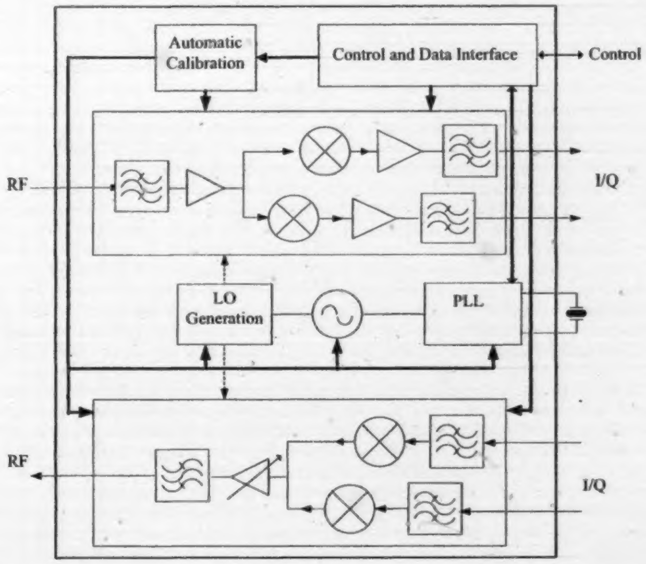


Figure 1-3: Block diagram of a general radio with built-in auto calibration and programmability to ensure high performance [10].

1.4.3.2 Software defined radios

The term software-defined radio (SDR) is usually used to refer to a radio transceiver in which key parameters are defined in software and in which the fundamental aspects of the radio operation can be reconfigured by upgrading that software [11]. Software defined radios are an enabling technology in areas such as military communications and civilian mobile communications. In military communications, an adaptable radio, which can change its scrambling codes, modulation format, and data rate on an ad hoc basis, can be adapted to harsh operational requirements. In civilian mobile communications, the cost of evolving a complete network to a new standard, by means of hardware replacement, is enormous. If the network infrastructure hardware is designed on software defined radio principles, the cost can be greatly reduced [11].

1.5 Typical specifications of RF front end building blocks

An accurate design at the system level is needed in order to meet the requirements of modern wireless systems. The main technical design requirements of radio receivers include frequency plan, sensitivity, and selectivity. A spreadsheet is usually used to model the cumulative gain, noise figure, and third-order intercept point in order to achieve optimum receiver performance. The individual specifications of each receiver block can then be deduced.

1.5.1 Noise figure

One parameter used to measure system noise performance is the noise factor *F*, the ratio of the signal-to-noise power ratio $(SNR)_{in}$ at the input of the system to the signal-to-noise power ratio $(SNR)_{out}$ at the output of the system, namely:

$$F = \frac{(SNR)_{in}}{(SNR)_{out}}. \tag{1.1}$$

The noise factor is a measure of the degradation in signal-to-noise ratio that a system introduces. The larger the degradation, the larger the noise factor [8]. When *n* matched blocks are cascaded, the total noise factor is given by the Friis formula:

$$F_{Cascaded} = F_1 + \frac{F_2 - 1}{G_1} + \ldots + \frac{F_n - 1}{\prod_{i=1}^{n-1} G_i}, \tag{1.2}$$

where G_i is the available power gain of each block. As seen from the Friis formula, the first stage in a cascade is the most critical in noise performance since the noise contributed by each stage decreases as the gain preceding the stage increases. The noise factor expressed in decibels (dB) is called noise figure.

1.5.2 Sensitivity

Sensitivity is an important design parameter of an RF receiver. The sensitivity of an RF receiver is defined as the minimum required signal-to-noise ratio at the input of the receiver to get a sufficient signal-to-noise ratio at the receiver output. The receiver sensitivity can be given by [7]:

$$S(dBm) = N + CNR + NF, \tag{1.3}$$

where S is the receiver sensitivity in dBm, N is the RF receiver noise floor, NF is the cascaded noise figure, and CNR is the required carrier-to-noise ratio at the receiver output to meet a minimum bit error rate (BER) requirement of a certain communication standard. It can be seen from equation (1.3) that lowering the noise figure of an RF receiver directly improves the sensitivity of a receiver and hence its ability to detect weaker signals. Since the LNA is the first block in a superheterodyne receiver, reducing the LNA noise factor is crucial for increasing RF receiver sensitivity.

1.5.3 Radio frequency receiver dynamic range

The power of the signals intercepted by a radio receiver varies over a wide range. The radio signal power is low when the receiver is far from the source of the received signals; the signal power increases when the receiver is close to the transmitter. The medium located between the receiver and the transmitter also affects the received signal strength. The term *dynamic range* defines a receiver's ability to accommodate signals with various power levels. The lower bound of the dynamic range is the receiver sensitivity as described in section 1.5.1. The upper bound is defined by the receiver linearity described in the following section.

1.5.3.1 Linearity

All real-life linear systems exhibit some degree of nonlinearity. The input-output characteristics can be modeled by the Taylor series expansion [7]:

$$v_o = a_0 + a_1 v_i + a_2 v_i^2 + \ldots = \sum_{n=0}^{\infty} a_n v_i^n , \tag{1.4}$$

where

$$a_n = \frac{1}{n!}\cdot\left(\frac{d^n v_0}{dv_i^n}\right)_{v_i=0}. \tag{1.5}$$

The input and output of the system are represented by v_i and v_o respectively. The coefficients a_n are assumed to be frequency independent. The output DC offset level is represented by a_0. The first order term, i.e. the amplified signal, is $a_1 v_i$. The term $a_2 v_i^2$ is the second-order (square-law) term, which contributes to the distortion as well as to other high order terms. Many linearity related problems can be analyzed by substituting v_i in equation (1.4) with:

$$v_i = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t. \tag{1.6}$$

The result will have terms at the fundamental input frequencies ω_1 and ω_2 as well as at harmonics of the fundamental frequencies. Of particular interest are the third-order products at the harmonic frequencies $2\omega_1\text{-}\omega_2$ and $2\omega_2\text{-}\omega_1$, illustrated in Figure 1-4 [8].

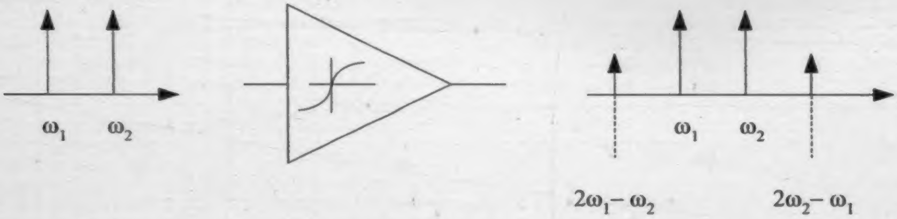


Figure 1-4: Intermodulation in a nonlinear system.

The importance of third-order products stems from the fact that if the difference between frequencies ω_1 and ω_2 is small, the components at frequencies $2\omega_1\text{-}\omega_2$ and $2\omega_2\text{-}\omega_1$ appear in the vicinity of ω_1 and ω_2. The corruption of signals due to third-order products is characterized by a performance metric called the "third-order intercept point" (IP3). IP3 is found by applying the two signals given by equation (1.6) to the input of a non linear system. As the amplitude of the two sinusoidal tones at ω_1 and ω_2 is increased, the third-order intermodulation (IMD) product will increase. IP3 is the point at which the amplitude of the third-order IMD would become equal to that of the fundamental. The input level at which this equality occurs is called the input third-order intercept point (IIP3) as illustrated in Figure 1-5.

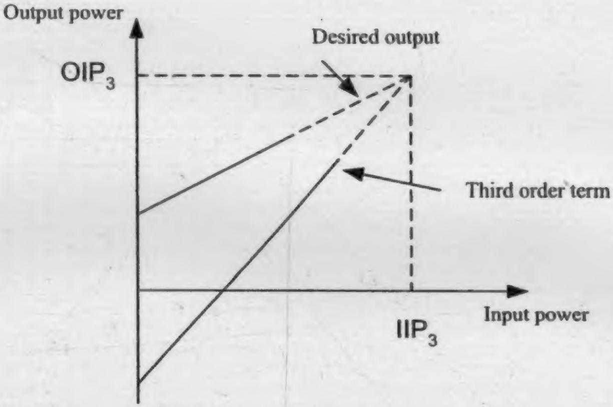


Figure 1-5: Definition of Linearity Parameters.

For a system including several cascaded blocks, the cascaded *IIP3* can be given by [9]:

$$\frac{1}{IIP3_{cascaded}} = \frac{1}{IIP3_1} + \frac{1}{IIP3_2/G_1} + ... + \frac{1}{IIP3_n/G_1..G_{n-1}}, \tag{1.7}$$

where $IIP3_n$ is the input intercept point of each stage and G_n is the gain of each stage respectively. The IMD products generated by a third-order nonlinearity can be given by:

$$IMD = 3 * P_{in} - 2 * IIP3, \tag{1.8}$$

where P_{in} is the magnitude of the input signal and *IIP3* is the third-order intercept point. The upper end of the dynamic range is the two tone signal level at which the IMD distortion product rises to the noise floor level and the lower end of the dynamic range is defined by the receiver sensitivity. Such a definition of the dynamic range is called the "spurious free dynamic range" (SFDR). The spurious free dynamic range represents the maximum level of interference that a receiver can tolerate while producing an acceptable signal quality from a small input level signal [7]. From equation (1.7) it can be seen that in order to increase the radio receiver linearity, higher gain stages should be the last stages in a cascade. To reduce receiver noise figure, higher gain stages should be placed at the beginning of the cascade. The distribution of gain over receiver stages directly affects the receiver dynamic range. In this thesis, the focus is on increasing a radio frequency dynamic range by lowering the receiver noise floor.

1.5.4 Oscillator phase noise

In an ideal oscillator, the frequency spectrum assumes the shape of an impulse; for an actual oscillator, the spectrum skirts around the carrier frequency. In specifying phase noise, the value of the noise power in a 1 Hz bandwidth at an offset frequency Δf from the carrier is measured. The phase noise is given by the normalized value of this measured noise power relative to the carrier power.

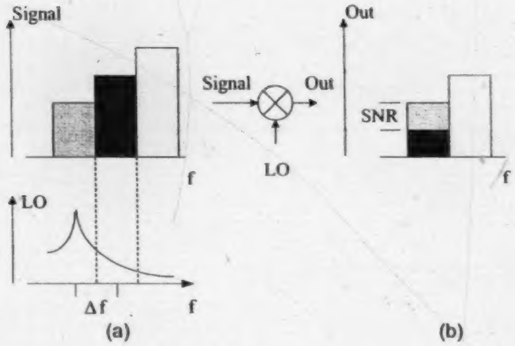


Figure 1-6: (a) Down conversion by an ideal oscillator; (b) Effect of phase noise on the down converted signal [12].

The effect of phase noise on RF receiver performance is shown in Figure 1-6 [12]. In an ideal oscillator, the signal of interest is mixed with an impulse representing the local oscillator and thus translated to a lower frequency with no change in shape. In reality, an interferer may accompany the desired signal and the local oscillator will exhibit finite phase noise. The down converted interferer can mask the desired down converted signal. Oscillator phase noise puts limitations on channel spacing. In phase modulated digital systems such as the global system for mobile communications (GSM), the phase noise of the synthesizer contributes to phase errors in the demodulated GSM signal constellation diagram. These deviations in the constellation points, which can be directly correlated to the LO phase noise, contribute to an increase in a system bit-error-rate (BER). Reducing phase noise leads to the efficient use of the frequency spectrum and to an increase in the user's capacity. Phase noise specifications for some of the most common modulation schemes are listed in Table 1-1.

Table 1-1: Typical Phase Noise Specifications for Digital Radio.

Standard	**Phase Noise**
BPSK	-85 dBc/Hz @100kHz
QPSK	-90 dBc/Hz @100kHz
16 QAM	-90 dBc/Hz @10KHz

Chapter 2

High Frequency Noise in Linear Two-Ports

2.1 Introduction

Deep submicron metal-oxide-semiconductor field-effect transistors (MOSFETs) are limited by the lack of RF noise models. Initial MOSFETs' noise models were developed for long channel MOSFET devices [8], [13]. Preliminary considerations show that short channel devices exhibit noise characteristics different from the predictions of the long channel theory [8]. To characterize the RF noise of MOSFET performance, scattering (S) parameters and noise parameters are required. Noise parameters include the minimum noise figure F_{min}, equivalent noise resistance (R_n), and an optimized source reflection coefficient (Γ_{opt}). After the S-parameters and noise parameters are determined, several other steps are required to develop MOSFET RF frequency noise models. These extra steps include extraction of a MOSFET small-signal model, de-embedding of noise parameters, and extraction of MOSFET noise sources. In addition, many parasitics such as probe pads and metallization surround the device under test (DUT). In order to obtain characteristics of the intrinsic transistor, the effect of these parasitics must be deembeded from the measured S-parameters and noise parameters. This chapter describes the steps required to extract MOSFET high frequency (HF) noise sources. A small-signal MOSFET model suitable for RF applications is presented in Section 1. Noise theories of noisy linear two-ports are presented in Section 2. The current noise models of CMOS transistors are reviewed in Section 3. Finally, a mechanical tuner-based noise parameter measurement setup is presented in Section 4.

2.2 MOSFET RF Model

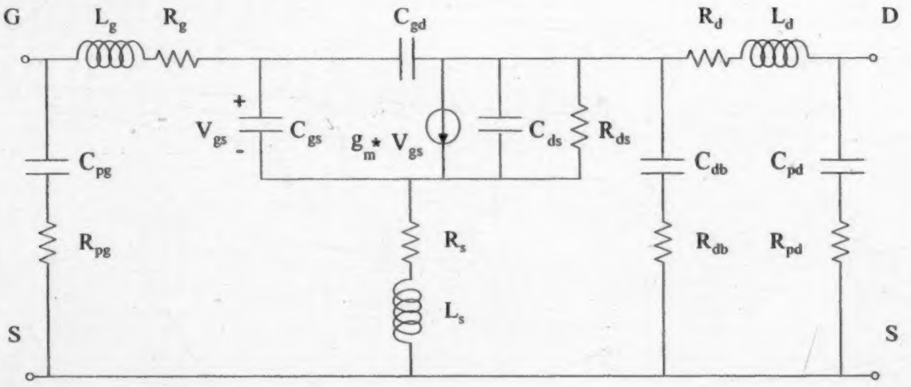


Figure 2-1: MOSFET small-signal model.

The equivalent circuit shown in Figure 2-1 is used to model the MOSFET small-signal electrical behavior at RF frequencies [14]–[17]. The MOSFET RF small-signal model can be divided into two parts: an extrinsic part and an intrinsic part. The extrinsic part includes elements that characterize parasitics surrounding the device such as the resistance of the silicided polysilicon gate (R_g), the source (R_s) and drain (R_d) junction resistances; the parasitic inductances of the gate, source, and drain metallization are given by L_g, L_s, and L_d, respectively. The two-element equivalent circuit formed by C_{db} and R_{db} represent losses in the conductive substrate. The intrinsic parts include the electrical elements that characterize the core of the metal oxide semiconductor (MOS) device. The channel capacitances are given by C_{gs} and C_{gd}; C_{ds} is the drain source capacitance; g_m is the device transconductance; R_{ds} is the output conductance; V_{gs} is the gate source voltage. The gate and drain pad capacitances are given by C_{pg} and C_{pd}, respectively.

2.2.1 Parasitic resistances and parasitic inductances

The noise performance of MOSFET transistors at RF frequencies is mainly affected by the parasitic components surrounding the device [17]. R_s and R_d account for the contact resistance between the source and drain junctions and the bulk substrate. The source and drain series resistances include any resistances between the metal electrodes at the source and drain and any other resistances leading to the MOSFET active channel. R_s and R_d in a MOSFET have several components such as via resistance, silicide resistance, silicide to silicide contact resistance, and sheet resistance in the lightly doped drain (LDD) region [17]. At low frequency, the gate resistance R_g results from the resistance of the silicided gate material. At RF frequencies, two other processes affect the value of the gate resistance. The first process is the distributed transmission line effect on the gate and the other process is the distributed effect on the channel [17]. The importance of correct modeling of R_g stems from the fact that it affects the match of the MOSFET to the driving source impedance and hence affects the noise figure as will be shown in Section 2.3. Values of the three parasitic resistances are in the order of a few ohms. The values of the parasitic resistances can be estimated from the S-parameters measurement done on a device with a gate source voltage (V_{gs}) and a drain source voltage (V_{ds}) equal to zero as will be shown in the next chapter.

The parasitic inductances L_g, L_s, and L_d are usually formed by the metallization connecting the metal oxide semiconductor (MOS) device to the pad. These inductances may also include the bond wire parasitics in case of a packaged device. The reactance of any metal contacts may also be included in the value of the parasitic inductances. The values of this inductance are layout dependent and usually range from zero to hundreds of picohenry (pH). For each device under test (DUT) designed for this thesis, the metallizations connecting the pads to the DUT were carefully designed in order to reduce the effects of the metallization impedance as will be shown in Chapter 3.

2.2.2 Intrinsic capacitances

The intrinsic capacitances shown on the equivalent circuit of Figure 2-1 include C_{gs}, C_{gd}, and C_{ds}. The capacitances C_{gs} and C_{gd} model the variations of channel charge density with respect to the gate-source and gate-drain voltages, respectively. The parasitic capacitances in a MOSFET can be divided into several fringing and overlap components [16] and [17]. These overlap and fringing capacitances are included in the final values of C_{gs} and C_{gd}. Variations of values of C_{gs} and C_{gd} with bias present an option to realize varactors. The drain source capacitance C_{ds} is included in the equivalent circuit to account for capacitance effects between source and drain electrodes.

2.2.3 Transconductance

The MOS device transconductance provides the intrinsic gain. A common measure for the gain efficiency of a MOSFET is its transconductance (g_m) per drain current g_m/I_{ds}, where I_{ds} is the drain source bias current [16]. MOSFETs require a large width/length (W/L) ratio and a high DC .biasing current to offer a transconductance comparable to the transconductance of a bipolar transistor biased with similar bias current. As MOSFET processing improves, and the gate dielectric thickness is reduced, the g_m/I_{ds} ratio has been found to improve [6]. The slope of the I_{ds}-V_{gs} characteristics can give the transconductance with the drain source voltage held constant. The transconductance g_m can be defined as:

$$g_m = \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{vds=constant} . \tag{2.1}$$

2.2.4 Output conductance

The resistance between the drain and source R_{ds} is usually presented in terms of its reciprocal, the output conductance, g_{ds}. The slope of the I_{ds}–V_{ds} characteristics can give the MOSFET output conductance with the gate source voltage held constant:

$$g_{ds} = \frac{1}{R_{ds}} = \left. \frac{\partial I_{ds}}{\partial V_{ds}} \right|_{vgs=constant} . \tag{2.2}$$

The device output conductance plays an important role in RF design as the value of this conductance determines the device gain and the output matching conditions needed to extract maximum power from a device operating as an RF power amplifier. In general, low values of g_{ds} are required in RF circuit design [16].

2.2.5 Substrate network

Modeling the substrate with a lumped equivalent circuit is a complicated task due to the distributed nature of the substrate. Several lumped equivalent circuits are presented [17] for modeling the MOSFET substrate network. Five-resistor networks were suggested in [18], four-resistor networks were proposed in [19], and Cheng *et al.* proposed three-resistor networks [19]. Two-resistor networks and one-resistor networks were proposed in [20]. The four- and five-resistor networks are more accurate and can be valid up to high frequencies, but analysis and extraction of equivalent circuit components is complex. Despite the fact that one- and two-resistor networks might be less accurate as the operating frequency is increased, these types provide easier analysis and parameter extraction.

2.3 Noise theory of linear two-port networks

Research on topics related to noise dates back to the early days of the past century [21]. For the noise theory of a linear two-port, the main contributions are presented in [22] and [23]. Results show that when the overall input-output noise behavior of a linear two-port network is considered, it is unnecessary to keep track of all the internal physical noise sources. A noiseless two-port that includes two correlated external noise sources can then model a linear noisy two-port. Depending upon the location and type (voltage or current noise source) of the external noise sources, two types of representations can be distinguished.

2.3.1 Representation of a noisy two-port using correlated noise sources

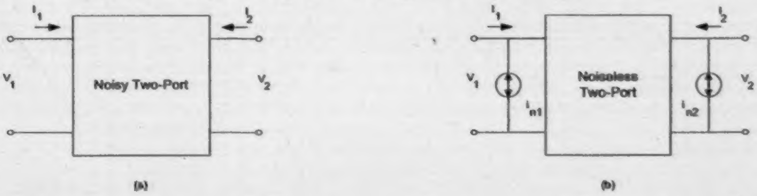
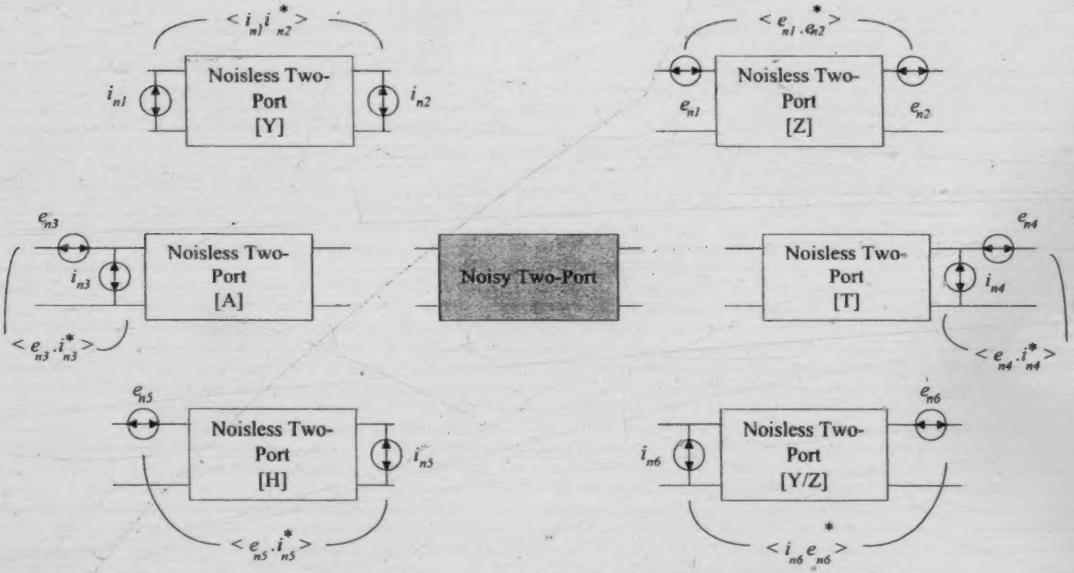


Figure 2-2: (a) Noisy two-port; (b) Noiseless two-port with two current sources placed at the input and output of the two-port network.

Haus and Adler [22] proved that a noisy two-port network is equivalent to a noiseless two-port network associated with a pair of correlated noise sources. The correlation coefficient is a measure of the way the two noise sources depend on each other. The noise sources could either be partially or totally correlated as they model the contribution from all the physical noise sources in the noisy two-port. The two noise generators could be either voltage sources or current sources or a combination of voltage and current. The sources could be placed at either the input or the output port of the two-port network [24]–[26]. For the noisy linear two-port shown in Figure 2-2, relations between input and output voltages and current can be represented by any set of linear two-port parameters such as impedance [Z] parameters or admittance [Y] parameters. Then the internal noise sources can be represented by two external correlated noise sources. The matrix representation of the two-port in Figure 2-2 using admittance parameters is [24]:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} i_{n1} \\ i_{n2} \end{bmatrix}, \tag{2.3}$$

where i_{n1} and i_{n2} are the noise sources at the input and output ports in admittance two-port parameters, and I_i and V_i are current and voltage, respectively, at the *i-th* port. Using the network theory for two-port electric circuits, six possible electrically equivalent representations for the noisy two-port can be constructed as shown in Figure 2-3 [24].



$<i_{n1} i^*_{n2}>$
i_{n1}
Noisless Two-Port [Y]
i_{n2}
$<e_{n1} . e^*_{n2}>$
e_{n1}
Noisless Two-Port [Z]
e_{n2}
e_{n3}
i_{n3}
Noisless Two-Port [A]
$<e_{n3} . i^*_{n3}>$
Noisy Two-Port
Noisless Two-Port [T]
e_{n4}
i_{n4}
$<e_{n4} . i^*_{n4}>$
e_{n5}
Noisless Two-Port [H]
i_{n5}
$<e_{n5} . i^*_{n5}>$
e_{n6}
i_{n6}
Noisless Two-Port [Y/Z]
$<i_{n6} e^*_{n6}>$

Figure 2-3: Six equivalent representations of a noisy two-port [24].

2.3.2 Representation of a linear two-port using four noise parameters

In 1956, Rothe and Dahlke introduced a new representation of a two-port using noise parameters [23], [27]. In this representation, a formula is derived to calculate the noise factor using four noise parameters. Internal physical noise sources can be replaced by a hypothetical correlated current source and a voltage source placed at the input of the noiseless two-port. The noiseless two-port is then driven by a current source with admittance Y_s as shown in Figure 2-4.

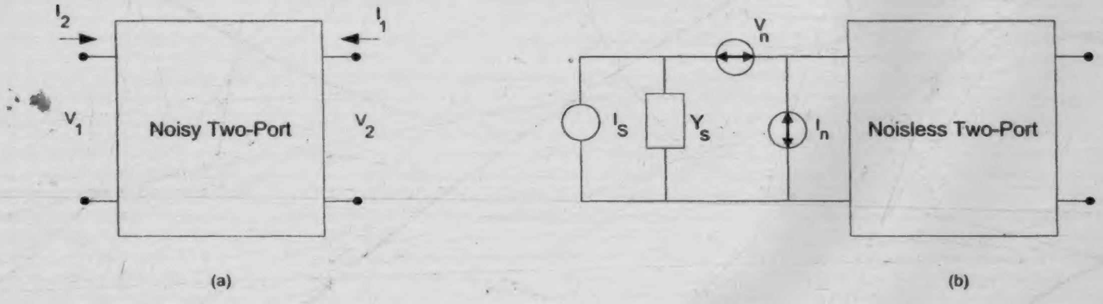


Figure 2-4: a) Noisy two-port; b) Equivalent noise model.

The noise factor of the linear two-port shown in Figure 2-4 can be given by equation (2.4) [27]:

$$F = F_{\min} + \frac{r_n}{g_s}\left|y_s - y_{opt}\right|^2, \tag{2.4}$$

where $y_s = Y_s/Z_0$ is the normalized admittance of the source driving the two-port given by:

$$y_s = g_s + jb_s, \tag{2.5}$$

where Y_s is the source admittance, Z_o is the characteristic impedance, g_s is the source conductance, and b_s is the source susceptance. F_{min} is the minimum noise factor that the network can achieve, and y_{opt} (g_{opt}, b_{opt}) is the normalized source admittance that produces the minimum noise factor. The coefficient r_n is the normalized noise resistance. The coefficient r_n determines the noise figure degradation when the generator admittance y_s deviates from the optimum value y_{opt}. The admittances y_{opt} and y_s can be expressed in terms of reflection coefficients Γ_s and Γ_{opt} using:

$$y_s = \frac{1-\Gamma_s}{1+\Gamma_s}, \tag{2.6}$$

and

$$y_{opt} = \frac{1-\Gamma_{opt}}{1+\Gamma_{opt}}. \tag{2.7}$$

Here Γ_s is the reflection coefficient of the source driving the two-port and Γ_{opt} is the source reflection coefficient that produces the minimum noise factor. Thus the noise factor can be given by [27]:

$$F = F_{\min} + 4r_n \frac{\left|\Gamma_S - \Gamma_{opt}\right|^2}{\left|1+\Gamma_{opt}\right|^2\left(1-\left|\Gamma_S\right|\right)^2}. \tag{2.8}$$

The main outcome of Rohde and Dahlke's theory is that four noise parameters F_{min}, r_n, and y_{opt} (Γ_{opt}) completely characterize linear two-ports from the point of view of noise.

From equation (2.8) it is seen that in addition to internal noise sources, the impedance of the generator driving the linear system affects the noise figure of a linear system. Equation (2.8) determines the initial guidelines for low noise design of a linear two-port. First, a device with low F_{min} and small value r_n should be chosen. Then the value of the generator admittance y_s should be close to y_{opt}. IC designers favor the two-port noise model presented in section 2.3.1 as this model allows calculation of the noise contribution of each element of the small-signal model of a MOS device. The second two-port noise model is mainly useful for designs using discrete components, as this model does not give an insight about the noise contribution of individual elements of a device.

2.4 Physical noise sources in MOSFETs

A simplified RF small-signal equivalent circuit of a MOSFET including noise sources is shown in Figure 2-5 [28]. The main noise source is the drain current noise $\overline{i_d^2}$ originating from the random motion of free carriers in the channel formed between source and drain. The drain current fluctuations cause an induced gate noise $\overline{i_g^2}$. Since they are originating from the same source, the gate noise and the drain noise are partially related by a correlation coefficient *C*. At RF frequencies, $\overline{i_G^2}$, $\overline{i_S^2}$, and $\overline{i_D^2}$ model the noise current generated by MOSFET gate, source, and drain resistances, respectively. The current noise source $\overline{i_{DB}^2}$ models the noise generated by the substrate resistance.

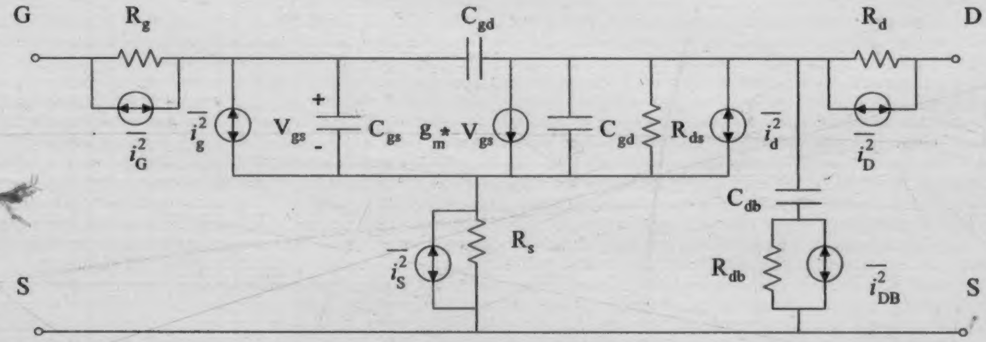


Figure 2-5: Noise equivalent circuit of MOSFET [28].

2.4.1 Thermal noise in MOS transistors

2.4.1.1 Drain current noise

Van der Ziel models the drain current thermal noise of long channel MOSFET transistors by [29]:

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f, \tag{2.9}$$

where k is Boltzmann's constant, T is the absolute temperature in Kelvin, Δf is the noise bandwidth in Hertz; g_{do} is the drain-source conductance at zero drain source voltage and can be given by:

$$g_{d0} = \left.\frac{\partial I_d}{\partial V_{ds}}\right|_{V_{ds}=0}. \tag{2.10}$$

For long channel devices, the parameter γ has a value of unity at zero V_{ds} and decreases toward a value of (2/3) in saturation. In short channel device models, a significant portion of the channel is velocity saturated and this affects the way the noise in the channel is modeled. A cross section of a short channel MOSFET is shown in Figure 2-6 [28]. The channel consists of two regions. Region I in Figure 2-6 is the gradual electron velocity region; region II in Figure 2-6 is the velocity saturation region. The channel length of region I is L_{elec} and the channel length of the saturation region (II) is ΔL. The applied drain to source voltage of region I is V_{dsat} and the total drain to source voltage is V_{ds}. $E_{crit.}$is the channel critical lateral electric field at which carriers travel at their saturation velocity v_{sat}.

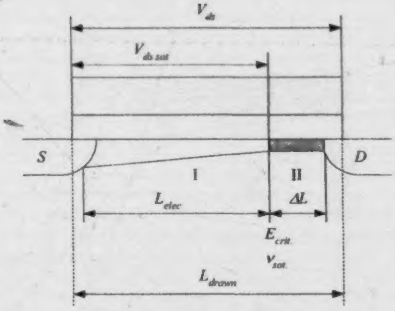


Figure 2-6: Cross-section of a MOSFET channel divided into a gradual channel region (I) and a velocity saturation region (II) [28].

Several models presented in the literature account for the impact of velocity saturation and the impact of carrier heating on the drain current noise in short channel devices. In these models, the factor γ was found to be variable with different device channel lengths and its values for short channel devices can be larger than the values for long channel devices owing to both velocity saturation and hot electrons. Contradicting values of γ were reported in the literature. For example, Abidi [30] indicated that the value of γ for short channel devices could be 3 to 4 times its long channel value. Chen [31] reported measured values of γ of MOSFET transistors with dimensions as low as 0.18 μm. The values of γ reported in [31] and [32] ranged from 1.1 to 1.8 for 0.18 μm MOSFETS with $W = 60$ μm (6 μm * 10 fingers) at a V_{ds} of 1.5 V and V_{gs} values of 0.7 V to 1.8 V. Scholten [33] reported measured values of γ close to the values reported by Chen and Deen [31], [32]. In addition to the controversies in calculating the values of γ, modeling the contribution of the noise generated in the velocity saturation region to the total thermal drain current noise differed among models [34]. For example, in the theory developed by Chen and Deen, the main contribution to the channel-generated noise was from region I and the velocity saturation region did not contribute to the drain current noise [35]. In [35], Chen clearly states that: *"However, in this thesis, we will show that there is no noise current generated from region II."* The analytical noise model presented in [35] used the channel length modulation (CLM) effect to calculate the channel noise of deep, submicron MOSFETs. The theory presented by Chen and Deen was verified by measurements on devices with gate lengths as low as 0.18 μm as mentioned earlier in this section. In the theory developed by Knoblinger *et al.* [36], noise generated by hot carriers in the velocity saturation region had a considerable effect on the noise generated in the channel. In [36], the authors state, "*It was found that considering hot carrier effects is essential for a correct simulation of the noise performance."* In [37] the authors state, *"Additionally, it is shown how the noise origin in the two transistor regions contribute to the total gate noise. In long channel transistors region II is neglected, with decreasing L, however, this part becomes more and more important."* The hot carrier effect was included in the model developed in [36] using an electric-field-dependent electron temperature. Results presented in [36] and [37] were experimentally verified on transistors with dimensions of 0.25 μm. Scholten [33] used a modified Klaasen-Pins integral method to prove that the entire channel contributed to the drain current noise. Results presented in [33] and [35] were verified by measurements on devices with dimensions as low as 0.13 μm.

2.4.1.2 Induced gate noise

At high frequencies, the fluctuating channel potential couples capacitively into the gate terminal, giving rise to noise current flowing to the gate [37], [34]. In the MOSFET RF noise model, besides the drain current noise $\overline{i_{nd}^2}$, an extra noise source $\overline{i_{ng}^2}$ (gate current noise) is introduced. The drain current noise $\overline{i_{nd}^2}$ and gate current noise $\overline{i_{ng}^2}$ are partially correlated. The gate current noise may be expressed as [38]:

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f, \tag{2.11}$$

Here the conductance g_g can be expressed as:

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}}, \tag{2.12}$$

where $\omega = 2\pi f$ is the operating frequency in radians per second and C_{gs} is the gate source capacitance. For long channel devices, Van der Ziel has shown that the gate noise coefficient δ has a value of twice γ in long channel devices. From equation (2.11), it can be seen that the induced gate noise is not a thermal noise source but has ω^2 dependence. In [37], a weak dependence of the induced gate noise on gate voltage was observed for transistors fabricated in a 0.25 μm technology. Random motion of free carriers in the MOSFET channel generate induced noise sources correlated with a correlation factor C defined in [39] and [40]:

$$C = \frac{\overline{i_g . i_d^*}}{\sqrt{\overline{i_g^2} . \overline{i_d^2}}}. \tag{2.13}$$

For typical radio frequencies, the real part of the correlation coefficient C is approximately equal to zero due to the purely capacitive coupling between the drain and gate noise generators [26]. For long channel devices, the imaginary part of the correlation coefficient has a value of 0.395 [26]. The sign of the imaginary part of the correlation coefficient depends on the drain and gate noise sources polarities [41], [42]. For short channel devices, the reported values of C were dependent on the dimensions of the device, but remained imaginary. Correlation coefficient values measured in [31] were in the range between 0.1 and 0.5 for a fixed device width of 60 μm and gate lengths varying from 0.18 μm to 0.97 μm at V_{gs} = 1.2 V and V_{ds} = 1 V. Correlation coefficient values reported in [33] had a negligible real part; values of the imaginary part were close to the values presented by Chen and Deen [31].

2.5 Flicker noise

Many of the performance problems that plague RF circuits are initially caused by flicker noise. For example, in voltage-controlled oscillators, flicker noise upconversion contributes to oscillator phase noise [17]. In current commutative mixers, flicker noise of the active devices appears at the output of the mixer at the baseband frequency which complicates the design of direct conversion receivers. The higher CMOS flicker noise represents an obstacle in implementing CMOS RF devices with similar noise performance to other competing semiconductor technologies. The precise sources of flicker noise in MOS devices are not yet known [17]. Three theories have been proposed in the literature to explain the origin of flicker noise [17]. In the carrier density fluctuation model, flicker noise is explained by fluctuation of channel-free carriers due to random capture and emission of carriers by interface traps at the silicon (Si) and silicon dioxide (SiO_2) interface. According to this model, flicker noise is fully defined by the number of interface traps and completely independent of gate bias, a claim that is not consistent with measurements performed on deep submicron transistors. A second theory is that fluctuations in carrier mobility are responsible for the generation of flicker noise. A third theory, a combination of the first two, suggests that the capture and emission of carriers by the interface traps cause fluctuations in both carrier numbers and carrier mobility, causing flicker noise. As MOSFET technology advances, more work is needed to substantiate these theories. For example, direct tunneling currents in ultra thin oxide transistors (e.g., 1.5 nm or less) may influence flicker noise [17]. Devices operating under switched bias conditions are of particular importance for RF circuit designers. The effects of the switching bias condition on flicker noise generation needs to be studied and included in existing flicker noise theories [17]. Lee [8] approximates the mean-square flicker drain noise current in NMOS devices by:

$$\overline{i_n^2} \approx \frac{K}{f}(2\pi f_t)^2 . A . \Delta f, \tag{2.14}$$

where A is the area of the gate, K is a device specific constant, f is the operating frequency, and Δf is the equivalent noise bandwidth.

2.6 Parasitic contribution to MOSFET thermal noise

At RF frequencies, in addition to channel thermal noise and induced gate noise, the parasitics surrounding the device contribute to the total thermal noise generated by the MOS device. Two important contributors are the gate resistance R_g and substrate resistance. The mean square noise voltage of the gate resistance can be given by:

$$\overline{v_g^2} = 4kTR_g\Delta f. \tag{2.15}$$

Several factors contribute to resistance of the gate including the finite resistivity of the silicided polysilicon and the resistance of the vias between the polysilicon and the bottom metal layer. In order to reduce the gate resistance R_g, multifinger layout is usually used. In the multifinger layout configuration, a device with large width (W) is divided into smaller parallel devices [43]. For a multifinger layout that uses contacts on one side of the fingers, the gate resistance is given by [43]:

$$R_g = \frac{W\rho_{poly}}{3N_f^2 L}, \tag{2.16}$$

where ρ_{poly} is the sheet resistance of the polysilicon gate material, W and L are the total width and length of the MOS device, and N_f is the number of parallel fingers. The factor 1/3 arises from a distributed analysis of the gate assuming each gate finger is contacted at only one end [41]. When each gate finger is contacted at both ends, this term is reduced to 1/12 [41]. The layout of an n-MOSFET with double-sided gate contact is shown in Figure 2-7. G, S, and D indicate the gate, source, and drain terminals respectively. W and L represent gate width and length respectively.

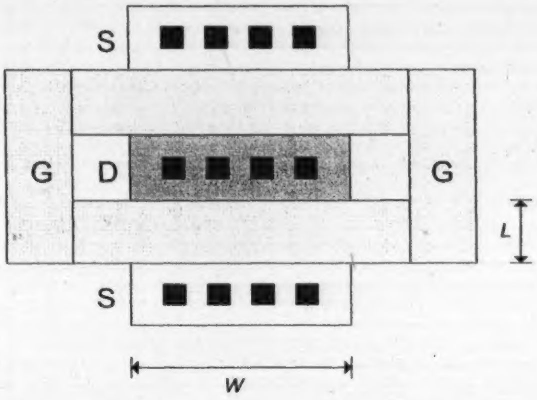


Figure 2-7: Layout of an n-MOSFET with double-sided gate contact.

Although equation (2.16) indicates that the gate resistance R_g can be reduced by increasing the number of fingers N_f, an increase in N_f leads to an increase in the gate to bulk parasitic capacitance which leads to a reduction in f_t, indicating a tradeoff between R_g and f_t [43]. The waffle layout method was proposed in [43] as a solution to the tradeoff associated with the traditional multifinger MOSFET layout. The waffle layout method allows the source/drain diffusion area to be shared by more transistor gates to reduce the total transistor active area and source/diffusion capacitances.

The thermal noise voltages produced by the substrate distributed resistance couple to the MOSFET channel causing fluctuations in channel current. Modeling of the substrate network is a challenging task as discussed in section 2.2.5. The reported contribution of the bulk resistance to the drain thermal noise varies in the literature [33]. In Scholten's [33] layout, where the device was surrounded with enough substrate contacts to minimize the value of R_{sub}, the substrate resistance contributed less than 3% of the total value of the drain current thermal noise. In [44], the substrate resistance added 25% more noise to the channel thermal noise.

2.7 Noise parameters calculation

In this section, an algorithm to calculate the noise parameters of the DUT in terms of the measured S-parameters and the available gain is presented [45] and [46]. The middle block shown in Figure 2-8 represents the DUT. S_b and G_b give the DUT S-parameters and available gain, respectively. The S-parameters and the available G define the passive devices placed at the input and output ports of the DUT. These passive devices include tuner, cables, and bias-tees. Γ is the reflection coefficient between blocks.

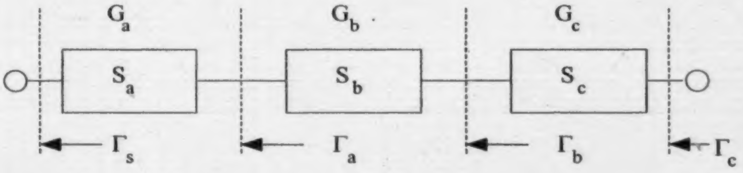


Figure 2-8: Effects of input and output blocks on noise parameters [45].

The reflection coefficients of the cascaded blocks can be given by [45]:

$$\Gamma_a = S_{22,a} + \frac{S_{12,b}.S_{21,a}.\Gamma_s}{1-\Gamma_s S_{11;a}}, \tag{2.17}$$

$$\Gamma_b = S_{22,b} + \frac{S_{12,b}.S_{21,b}.\Gamma_a}{1-\Gamma_a S_{11,b}}, \tag{2.18}$$

$$\Gamma_c = S_{22,c} + \frac{S_{12,c}.S_{21,c}.\Gamma_b}{1-\Gamma_b S_{11,c}}, \tag{2.19}$$

where Γ_s is the reflection coefficient of the noise source. The available gains can be expressed in terms of the reflection coefficients as [45]:

$$G_a = \frac{\left|S_{21,a}\right|^2\left(1-\left|\Gamma_s\right|^2\right)\left(1-\left|\Gamma_a^*\right|^2\right)}{\left|\left(1-\Gamma_s S_{11,a}\right)\left(1-\Gamma_a^* S_{22,a}\right)-\Gamma_s\Gamma_a^* S_{12,a}S_{21,a}\right|^2}, \tag{2.20}$$

$$G_b = \frac{\left|S_{21,b}\right|^2\left(1-\left|\Gamma_a\right|^2\right)\left(1-\left|\Gamma_b^*\right|^2\right)}{\left|\left(1-\Gamma_a S_{11,b}\right)\left(1-\Gamma_b^* S_{22,b}\right)-\Gamma_a\Gamma_b^* S_{12,b}S_{21,b}\right|^2}, \tag{2.21}$$

$$G_c = \frac{\left|S_{21,c}\right|^2\left(1-\left|\Gamma_b\right|^2\right)\left(1-\left|\Gamma_c^*\right|^2\right)}{\left|\left(1-\Gamma_b S_{11,c}\right)\left(1-\Gamma_c^* S_{22,c}\right)-\Gamma_b\Gamma_c^* S_{12,c}S_{21,c}\right|^2}. \tag{2.22}$$

Using equations (2.17)–(2.22), the noise factor of the DUT can be given by [45]:

$$NF_b = G_a\left(NF_m - NF_a - \frac{NF_c - 1}{G_a G_b}\right)+1, \tag{2.23}$$

where NF_a and NF_c are:

$$NF_a = \left(\frac{1}{G_a}-1\right)\frac{T}{T_0}+1, \tag{2.24}$$

$$NF_c = \left(\frac{1}{G_c}-1\right)\frac{T}{T_0}+1, \tag{2.25}$$

where T_0 = 290 K. NF_m denotes the noise figure of a cascaded system, and NF_k and G_k represent the noise figure and available gain, respectively, of the *k*th two-port. After deembeding the measured noise parameters, the four noise parameters can be extracted by the solution of an over-determined linear system of equations in a method proposed by Lane [46]. The solution is obtained by rearrangement of equation (2.8) into the linear form:

$$\mathrm{Re}\left\{Y_{s,i}\right\}NF_i = \left|Y_{s,i}\right|^2 x_i - 2\,\mathrm{Im}\left\{Y_{s,i}\right\}x_2 + x_3 + \mathrm{Re}\left\{Y_{s,i}\right\}x_4, \tag{2.26}$$

where NF_i and $Y_{s,i}$ represent the noise figure and the source admittance of the DUT for the i_{th} measurement. Re{} and Im{} represent real and imaginary parts of the parameters in braces. The four unknowns can be given by solving the following set of equations:

$$x_1 = R_n, \tag{2.27}$$

$$x_2 = \mathrm{Im}\left\{Y_{s,opt}\right\} R_n, \tag{2.28}$$

$$x_3 = \left|Y_{s,opt}\right|^2 R_n, \tag{2.29}$$

$$x_4 = F_{\min} - 2\,\mathrm{Re}\left\{Y_{s,opt}\right\} R_n. \tag{2.30}$$

The four noise parameters can be obtained by inversion of equations (2.27)–(2.30) [45]:

$$R_n = x_1, \tag{2.31}$$

$$\mathrm{Im}\left\{Y_{s,opt}\right\} = \frac{x_2}{x_1}, \tag{2.32}$$

$$\mathrm{Re}\left\{Y_{s,opt}\right\} = \sqrt{\frac{x_3}{x_1} - \left(\frac{x_2}{x_1}\right)^2}, \tag{2.33}$$

$$F_{\min} = x_4 + 2\sqrt{x_1 x_4 - x_2^2}_{\;n}, \tag{2.34}$$

2.8 Noise parameters measurement system description

As seen from equation (2.8), the four noise parameters of the two-port can be fully determined from a set of noise figure measurements done by varying the source impedance seen by the input port of the DUT. Since there are four noise parameters, a minimum of four measurements have to be made. However, because of various uncertainties in noise parameter measurement, it is necessary to make significantly more measurements, typically twelve to sixteen [47]. A tuner is usually used to vary the impedance seen by the DUT.

Also, the S-parameters of the tuner, DUT, and all interconnecting blocks have to be known for accurate noise parameter calculation. A detailed block diagram of the noise measurement setup is shown in Figure 2-9.

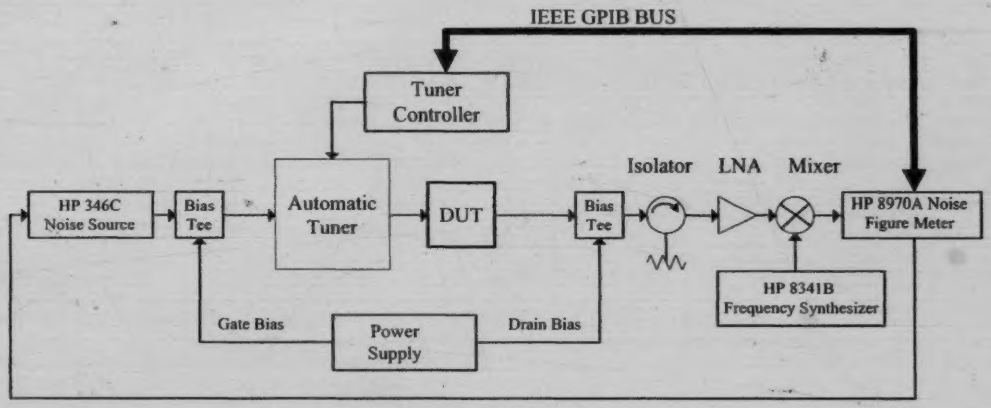

IEEE GPIB BUS
Tuner Controller
Isolator
LNA
Mixer
HP 346C Noise Source
Bias Tee
Automatic Tuner
DUT
Bias Tee
HP 8970A Noise Figure Meter
HP 8341B Frequency Synthesizer
Gate Bias
Power Supply
Drain Bias

Figure 2-9: Noise measurement system set up.

The measurement setup consists of a programmable tuner, a tuner controller, a vector network analyzer, a noise source, a frequency synthesizer, and a noise figure meter. All instruments are connected to a GPIB bus. DUT represents the device under test whose noise parameters will be measured. Input to the system is provided by the noise source. The output noise power is measured, processed, and displayed by the noise figure meter. The source tuner generates arbitrary, accurate reflection coefficients (Γ_s). As mentioned in section 2.7, a simplified method of noise measurement consists of using the source tuner to synthesize several Γ_s, while measuring the noise factor. Then, the four DUT noise parameters can be calculated from equations (2.31) – (2.34).

2.8.1 Tuners

The noise measurement setup used in this thesis is built around an automated tuner system provided by Maury Microwave Corporation [47]. Tuners can generate reflection coefficients by introducing controllable discontinuities on a transmission line. The tuner used in this setup is the MT982E. The MT982E is an electromechanical slide screw tuner with a frequency operating range of 0.8 to 8 GHz. In a slide screw tuner, a carriage that moves a probe along a transmission line generates the discontinuities. The probe can also move up or down toward the central conductor of the transmission line. In an automated tuner, stepper motors automate probe and carriage motions. The main benefits of an automated tuner over a manual tuner include accuracy and repeatability of impedance synthesis.

2.8.2 Noise figure meter and noise source

The Hewlett Packard (HP) 8970A noise figure meter measures the noise power at the output of the system. The HP8970 noise figure meter is a sensitive, tunable, automatic receiver with a frequency range from 10 – 1600 Hz. To extend the measurement frequency range of the HP8970A above 1.6 GHz, an external mixer (Mini-Circuits model ZX05-C60) is used to down convert the DUT output to the frequency range of the noise figure meter. A frequency synthesizer that can be controlled by the noise figure meter drives the mixer. The frequency synthesizer used in the noise measurement setup is the HP8341B. The frequency synthesizer covered a broad frequency range (10 MHz – 20 GHz) and provided adequate power outputs to drive the double balanced mixers used in the setup. A high gain, low noise preamplifier (LNA) (Mini-Circuits model ZX60-8008E) was placed in front of the passive mixer to reduce the effect of the mixer attenuation on the overall system noise figure. Both the LNA and the mixer were operating in their linear range. A directional coupler (HP779D) or an isolator can be inserted at the input of the noise figure meter. The role of the directional coupler or the isolator is to provide 50 ohms impedance to the noise receiver irrespective of the variations in the output impedance of the DUT. The noise parameter measurement methods discussed in section 2.7 require a noise source to be switched between two distinct temperatures. The noise source used in the setup is the HP346B. The HP346B is a solid-state noise source that uses an avalanche diode to generate random thermal broadband noise. The diode can be biased from a +28 VDC supply (found on the noise figure meter) to generate an output noise, which corresponds to a hot noise temperature (T_h). A cold noise temperature (T_c) corresponds to the physical temperature of the source when the bias is removed. These two noise levels are used to measure the gain and added noise figure of the device under test and, consequently, its noise figure.

2.8.3 Peripheral devices

Other devices used in the setup include a Tektronix power supply (model 2521G) for biasing the DUT. Unlike flicker noise measurements where batteries are used for bias, switch mode power supplies were used in the noise figure measurement set up. This is due to the fact that the 60 Hz noise generated by these power supplies does not fall in the operating frequency range of the noise measurement system (1–6 GHz). A Keithly multi meter (model 2001) was used to measure the drain current. The probes used were the GGB industries ground-signal-ground (GSG) 150 μm pitch on-wafer probes. A die fabricated in Taiwan Semiconductors Manufacturing Corporation's (TSMC) 0.18 μm technology was bonded to an aluminum substrate using conductive epoxy. The substrate was placed over a locally fabricated chuck connected to a vacuum pump. Detailed description of the die and the DUTs will be provided in chapter three. Maury Microwave software controls the network analyzer, tuner controller, noise figure meter, and the frequency synthesizer through a GPIB bus. The software synchronized the operation of the noise source, gathered measured noise power data from the noise figure meter, tuned the local oscillator frequency, and generated plots of the measured noise parameters.

2.8.4 Calibration and measurement procedure

Before starting the noise parameter measurements, several calibration steps are needed to successfully measure the S-parameters and noise parameters of the DUT.

1. Network analyzer calibration: In order to measure the S parameters of the different system components and the on-wafer DUT S-parameters, the network analyzer needs to be calibrated. Two different calibration standards were used according to the type of connectors in the device that needed to be calibrated. For devices with subminiature type A (SMA) connectors, the 8510B was calibrated with the calibration standards Short, Open, Load, and Thru (SOLT) using an HP calibration kit. For the on-wafer DUT S-parameter measurements, on-wafer coplanar SOLT standards built on GGB industries impedance standard substrates (ISS) were used. The ISS manufacturer provided the coefficients

defining each standard. These coefficients were loaded into the Vector Network Analyzer (VNA). A calibrated VNA is used to measure S-parameters of the DUT, bias tees, and all the components between the noise source and the noise receiver. S-parameters were measured using the HP8510B VNA. The HP8510B VNA includes the HP8516A S-parameters test set and the HP8341B synthesizer sweeper. The HP synthesizer sweeper provides the stimulus (frequency and power) to the DUT. The test set measures and separates incident and reflected waves from the DUT ports.

2. Tuner characterization: Tuner characterization consists of measured tuner two-port S-parameter data and corresponding tuner positions measured over the operating frequency range. The tuner characterization method selects positions with a constant separation on a Smith chart. Once tuner characterization is done, the tuner can be controlled to move to specific points on a Smith chart.

3. To characterize the contribution of the noise receiver to the total measured noise figure, the noise figure of the noise receiver has to be known. Using the Friis formula, the effect of the noise figure meter is deembeded from the DUT noise measurements. The noise parameters of the noise figure meter are measured over a number of preselected tuner positions. For the noise calibration, a Thru standard with known S-parameters replaces the DUT; complete noise and gain parameters of the receiver were measured versus frequency.

After the calibration procedure is terminated, the DUT is inserted in the setup and biased. The selection of the tuner impedances directly affects the noise figure measurement results

[48]. Some tuner impedances can produce ill-conditioned matrices in the set of equations needed to calculate noise parameters, which can lead to erroneous noise parameter results. Several methods for selecting source impedances have been reported in the literature. Van Den Bush and Martens [49] proposed distributing the tuner positions according to a constellation diagram in the shape of a cross as shown in Figure 2-10 [48]. In [49] it was determined that the orientation of the diagram largely affects the precision of the results. A two-step algorithm was proposed to improve the accuracy of the results. In the first step, five tuner impedances (1, 6, 7, 8, and 9 in Figure 2-10) are selected. Using these points, the position of the phase of Γ_{opt} can be approximately predicted. In the second step, four other points are selected that can analytically improve the noise parameters. A method proprietary to Maury Microwave suggests placing tuner impedances close to the area of a Smith chart where the complex conjugate of the DUT output reflection coefficient is located [47]. Also, Maury Microwave's software allows manual selection of tuner impedances. Over the course of noise parameter measurements done for this thesis, it was concluded that the three methods provided in [47] yield approximate results, and the point selection method proprietary to Maury Microwave was followed to produce the noise measurement results for this thesis. The linearity and stability of the DUT were observed during the noise measurement process. All the tuner positions were selected in the stable area determined by a stability circle over a Smith chart. Several algorithms for accurate determination of noise parameters have been suggested in the literature [49]–[51]. Escotte *et al.* [52] presented a comparative study on accuracy of the different algorithms used for noise parameter determination. The result of the study done in [52] indicated that

algorithms proposed by Boudiaf and Laporte [50] provided a slight improvement in accuracy of the measured noise parameters compared to the algorithms in [46] and [51].

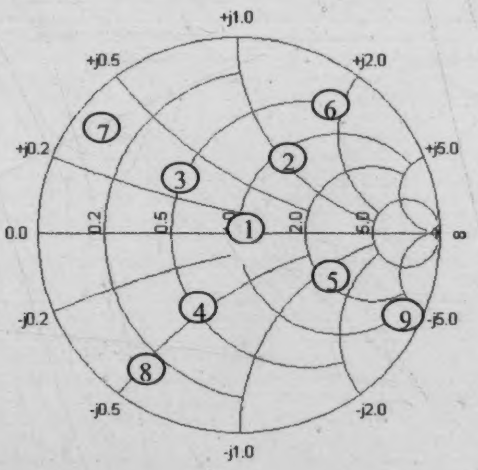


Figure 2-10: Impedance distribution on a Smith chart [48].

Chen and Deen used a system based on solid-state tuners provided by ATN Microwave, Inc. [32]. The ATN system provides a turn-key solution for complete S-parameter and noise parameter measurements. An advantage of this system is its speed in generating impedance points compared to a mechanical tuner; in the ATN tuner there are no mechanical parts. Another advantage is the light weight of the solid-state tuner. A lightweight tuner generates fewer vibrations, which makes it more suitable for on-wafer measurements. A drawback of the solid-state tuner is the limited ability to cover high reflection coefficient areas on a Smith chart. Wide tuner coverage on a Smith chart is required in cases where the value of r_n is low. As seen from equation (2.8), a low value of r_n causes a wider crux of the surface generated by equation (2.8), which renders the determination of F_{min} difficult. Scholten [33] used a local built noise parameter measurement system [53]. The system is based on an improved Y-factor method that accounts for the difference in the impedance of the noise source in the hot and cold states [33]. In this system, instead of a tuner, three precharacterized loads generate the required impedances for noise parameter measurements. Again, the advantage of this method is the speed of the system compared to a mechanical tuner-based system.

2.9 Conclusion

This chapter discusses small-signal RF modeling of MOSFETs. The origin of each element in the model was investigated to clarify factors affecting the element value. The model is composed of extrinsic elements that represent the parasitics surrounding the device and intrinsic elements that represent the device core.

Noise representation in a linear-two port was discussed. The various models describing the noise performance of RF MOSFETs are explained. Models that account for the impact of velocity saturation and carrier heating on the drain current noise of RF MOSFETs were described. A mechanical-tuner based set up to extract the noise parameters of MOSFET transistors operating at RF frequencies is described.

Chapter 3

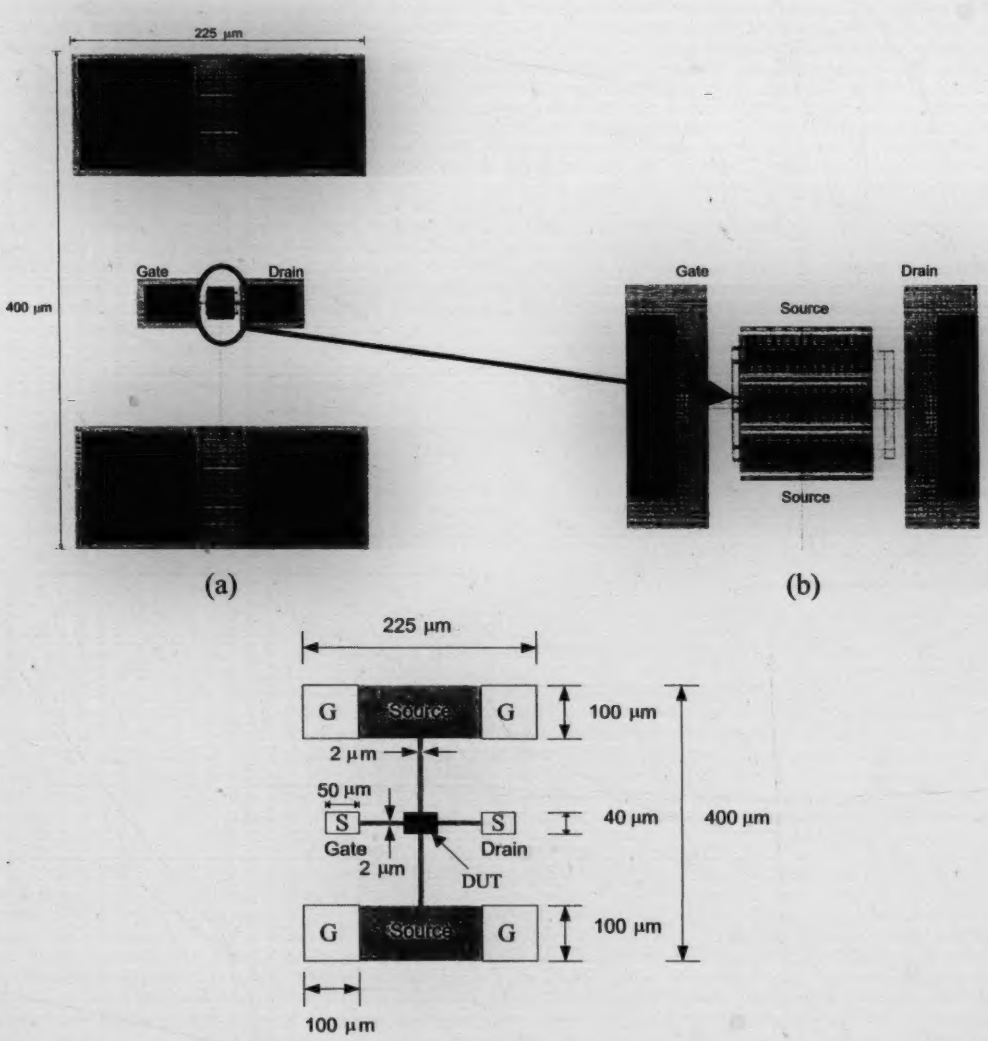
High Frequency Channel Noise Measurement and Characterization in Deep Submicron MOSFETs

3.1 Introduction

In Chapter 2 we addressed the steps needed for high frequency noise characterization of MOSFETs for RF IC applications. In this chapter we present the methodology of extraction of MOSFET small-signal parameters. In section 3.2 we evaluate several channel thermal noise models suitable for MOSFET devices operating at high frequencies. Measurements were done on NMOS devices with channel widths (*W*) of 120 μm (20 μm*6 fingers) and channel lengths (*L*) of 0.18 μm, 0.36 μm, and 0.54 μm. Comparison of extracted and calculated noise data indicates that a recently published simple model of short channel devices operating at RF frequencies provides the best match between extracted and calculated results for the channel thermal noise over a frequency range of 3 GHz to 6 GHz and a gate overdrive voltage range of 0.2 V to 1.2 V.

3.2 Test Transistors

3.2.1 MOS transistor layout


225 µm
400 µm
Gate
Drain
Gate
Drain
Source
Source
225 µm
G
Source
G
100 µm
2 µm
50 µm
S
S
40 µm
400 µm
Gate
Drain
2 µm
DUT
G
Source
G
100 µm
100 µm

(a)

(b)

(c)

Figure 3-1: (a) MOS transistor test structure; (b) MOS transistor layout; (c) MOS transistor test structure dimensions (not to scale).

The layout of the NMOS test structure is shown in Figure 3-1.a. The NMOS transitor layout is shown in the close-up of Figure 3-1.b. The test structure dimensions are shown Figure 3-1.c. A systematic procedure for transistor layout was followed. NMOS transistors were built using a unit 20 μm width device as shown in Figure 3-1. NMOS transistors operating at RF frequencies are usually designed with a smaller width in order to increase f_t [8]. In this thesis, the unit transistor width was chosen to avoid cross talk between the facing on-wafer probes [54]. The gate lengths of this unit transistor were varied. The gate lengths of the unit transistors were 0.18 μm, 0.36 μm, and 0.54 μm. Larger devices are built using several parallel unit transistors. The designed device widths are 120 μm. Two metal layers are used to make connections to the source and drain of the device under test (DUT). The bottom metal (metal 1) layer with a sheet resistance of 78 milliohms/square is used to connect to gate and drain terminals. Metal 2 with a sheet resistance of 78 milliohms/square was used for the source interconnection. Each test transistor contains 6 pads in a ground-signal-ground configuration. The transistors are connected in a common source configuration with the bulk connected to the source of the transistors. The metal connections from the source terminals to the ground pads were not shielded from the substrate. In the test structure shown in Figure 3-1.a, the width of the metal strip connecting the source terminals to the ground pads was selected as 2 μm. The metal strip has a resistance of 6 Ω. However, a wider width of the metal strip will reduce the metallization resistance in series with the source terminal. The die photograph of the designed transistors is shown in Figure 3-2. The passive devices used in de-embedding the pad parasitics are the open devices shown in section 3.2.2. The die layout of test transistors built in TSMC 0.18 μm technology is shown in Figure 3-2.

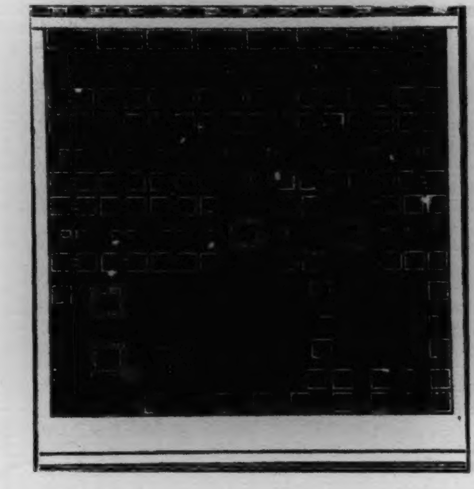


Figure 3-2: Die photograph of test transistors built using 0.18 μm technology. The die dimensions are 2000 μm × 2000 μm.

3.2.2 Pad equivalent circuit

An equivalent circuit that includes a capacitance and a resistance can model the RF pad [55]. The capacitance is formed between the pad metal and the conductive substrate. The pad resistance arises from losses in the conductive substrate. The values of pad capacitance are in the order of a few femto farads, while pad resistances are usually in the order of a few kilo ohms. The equivalent circuit model of the pad parasitics surrounding the DUT is shown in Figure 3-3. The elements Y_{p1}, Y_{p2}, and Y_{p3} represent the parasitics introduced by pads and the metallization surrounding the device. The effects of pad parasitic contributions to measured parameters of the DUT can be deembedded using the two-port theory as shown in section 3.2.3. An ideal RF pad has a small capacitance and a high resistance to ground. The design of an RF pad entails a trade-off between the minimum allowed pad area and the capability of the measuring on-wafer probes. The pad area needs to be as small as possible in order to reduce the capacitance to ground. However, the reduction of pad area is usually constrained by either the on-wafer probe tip minimum required area for proper on-wafer measurements or by the capability of the bonding machine. The pads were implemented without electrostatic discharge (ESD) protection.

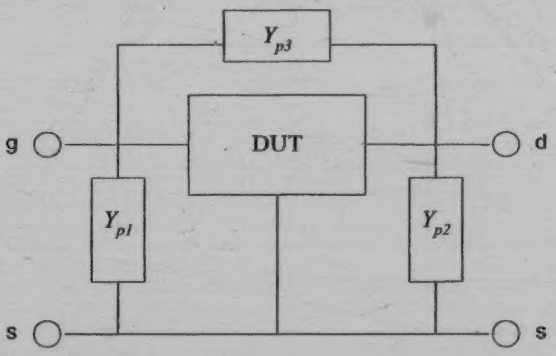


Figure 3-3: Equivalent circuit used for deembedding the effects of pads.

3.2.3 Methodology of extraction of MOSFETs' RF small-signal model

In the equivalent circuit shown in Figure 3-3, the gate terminal acts as port 1 and the drain terminal acts as port 2. Gate, drain, and source resistances can be extracted from the impedance (Z) parameters at a gate source voltage (V_{gs}) and a drain source voltage (V_{ds}) equal to zero [43] and [56]. These gate and drain bias values ensure that the contribution of the transconductances g_m and the output conductance g_{ds} are equal to zero. The gate, source, and drain resistances can be extracted using [56]:

$$\begin{aligned} \mathrm{Re}(Z_{11}) &= R_g + R_s, \\ \mathrm{Re}(Z_{12}) &= \mathrm{Re}(Z_{12}) = R_s, \\ \mathrm{Re}(Z_{22}) &= R_d + R_s. \end{aligned} \tag{3.1}$$

The parasitic resistances R_g, R_s, and R_d are assumed bias independent. The calculated parasitic resistances can be deembedded from the measured Z-parameters of a biased MOSFET. The deembedded admittance parameters (Y) of the biased MOSFET can be approximated by [56]:

$$Y_{11} \approx \omega^2 C_{gg}^2 R_g + j\omega C_{gg}, \tag{3.2}$$

$$Y_{12} \approx -\omega^2 C_{gd} C_{gg}^2 R_g - j\omega C_{gd}, \tag{3.3}$$

$$\begin{aligned} Y_{21} \approx g_m - \omega^2 C_{gd} C_{gg} R_g - j\omega C_{gd} \\ -j\omega g_m C_{gg} R_g, \end{aligned} \tag{3.4}$$

$$\begin{aligned} Y_{22} \approx g_{ds} + \frac{\omega^2 C_{db}^2 R_{db}}{1+\omega^2 C_{db}^2 R_{db}^2} + \omega^2 g_m C_{gd} C_{gg} R_g^2 + \\ j\omega\left(C_{ds} + C_{gd}\right) + j\omega \frac{C_{db}}{1+\omega^2 C_{db}^2 R_{db}^2} + j\omega g_m C_{gd} R_g, \end{aligned} \tag{3.5}$$

where C_{gg} is defined as the total capacitance given by:

$$C_{gg} = C_{gd} + C_{gs} + C_{gb}. \tag{3.6}$$

The Y-parameters given by equations (3.2)–(3.5) were calculated using the assumption $\omega^2 C_{gg}^2 R_g$ << 1. This assumption should be validated after extraction of the small-signal parameters. Then the elements of the small-signal MOSFET model can be extracted using the real and imaginary parts of equations (3.2)–(3.5) [55], [56]:

$$g_m = \mathrm{Re}(Y_{21})\big|_{\omega^2=0}, \tag{3.7}$$

$$g_{ds} = \frac{1}{R_{ds}} = \mathrm{Re}(Y_{22})\big|_{\omega^2=0}, \tag{3.8}$$

$$C_{gg} = \left|\frac{\mathrm{Im}(Y_{11})}{\omega}\right|, \tag{3.9}$$

$$C_{gd} = \left| \frac{\mathrm{Im}(Y_{12})}{\omega} \right|. \tag{3.10}$$

Modeling the substrate with a lumped equivalent circuit is a complicated task due to the distributed nature of the substrate [17]. Despite the fact that one- and two-resistor networks might provide less accurate models of the substrate as the operating frequency is increased, these types provide easier analysis and parameter extraction. After extracting the components R_{db} and C_{db}, the drain source capacitance C_{ds} can be extracted using [56]:

$$\begin{aligned} C_{ds} = {} & \frac{\mathrm{Im}(Y_{22})}{\omega} - C_{gd} - j\omega \frac{C_{db}}{1+\omega^2 C_{db}^2 R_{db}^2} \\ & - j\omega g_m C_{gd} R_g . \end{aligned} \tag{3.11}$$

In summary, the pad deembedding steps and the small-signal parameter extraction can be given by the deembedding stages shown in Figure 3-4 [57]:

- On-wafer measurement of the S-parameters of the extrinsic device
- Transformation of S-parameters to the admittance Y-parameters and subtraction of the effects of pad parasitics
- Transformation of Y-parameters to the impedance Z-parameters and subtraction of the effects of series resistances and inductances at the gate source and drain
- Transformation of the impedance parameters to Y-parameters to determine the intrinsic Y parameters of the device

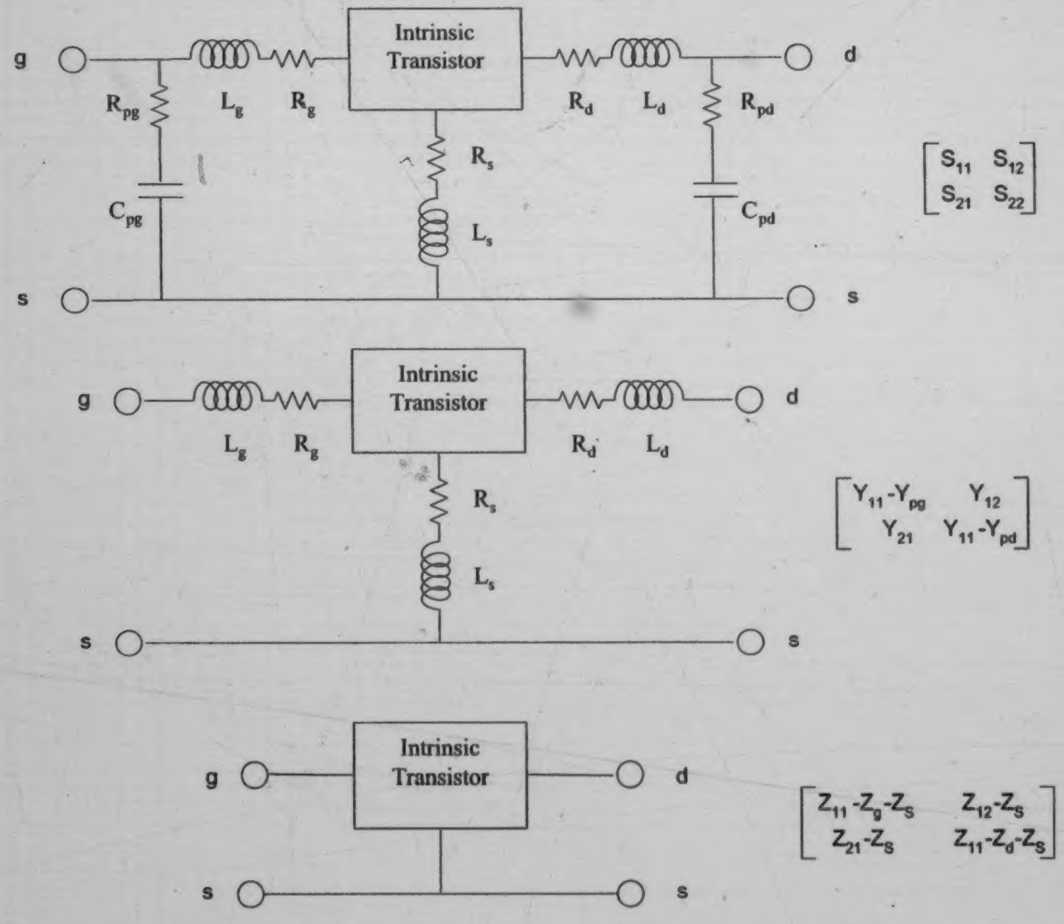

g
Intrinsic Transistor
d
R_{pg}
L_g
R_g
R_d
L_d
R_{pd}
R_s
C_{pg}
L_s
C_{pd}
s
s
$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$
g
Intrinsic Transistor
d
L_g
R_g
R_d
L_d
R_s
L_s
s
s
$\begin{bmatrix} Y_{11}-Y_{pg} & Y_{12} \\ Y_{21} & Y_{11}-Y_{pd} \end{bmatrix}$
g
Intrinsic Transistor
d
s
s
$\begin{bmatrix} Z_{11}-Z_g-Z_S & Z_{12}-Z_S \\ Z_{21}-Z_S & Z_{11}-Z_d-Z_S \end{bmatrix}$

Figure 3-4: Method of extracting MOSFET intrinsic parameters [57].

The substrate resistance and capacitance can be extracted using a simple two-elements model [55]. The extraction method using equations (3.7)–(3.11) was applied to extract the parameters of NMOS transistors fabricated in a TSMC 0.18 μm process. S-parameters were measured using an Agilent HP8150B vector network analyzer and on wafer probes over the frequency range (1–6 GHz). The measured and simulated S-parameters of an N-type MOSFET with channel width 120 μm and gate lengths of 0.18 μm, 0.36 μm, and 0.55 μm, biased at V_{gs} = 1.2 V and V_{ds} = 1.8 V are shown in Figure 3-5, Figure 3-6, and Figure 3-7, respectively. The S-parameters measurements were done at room temperature. As shown from figures 3-5, 3-6, and 3-7, good agreement was found between measured and simulated S-parameters. The small-signal model parameters at 5 GHz of an N-type MOSFET with channel width 120 μm and gate length 0.54 μm, biased at V_{gs} = 1.2 V and V_{ds} = 1.8 V are given by: g_m = 0.03911 S, r_{ds} = 464 Ω, C_{gs} = 462 fF, C_{gd} = 39 fF, C_{ds} = 171 fF, R_d = 11 Ω, R_s = 6 Ω, R_g = 13 Ω, C_{db} = 153 fF, and R_{db} = 430 Ω. Discrepancies between the measured and simulated output reflection coefficients might be due to the simple two-elements model used to represent the substrate.

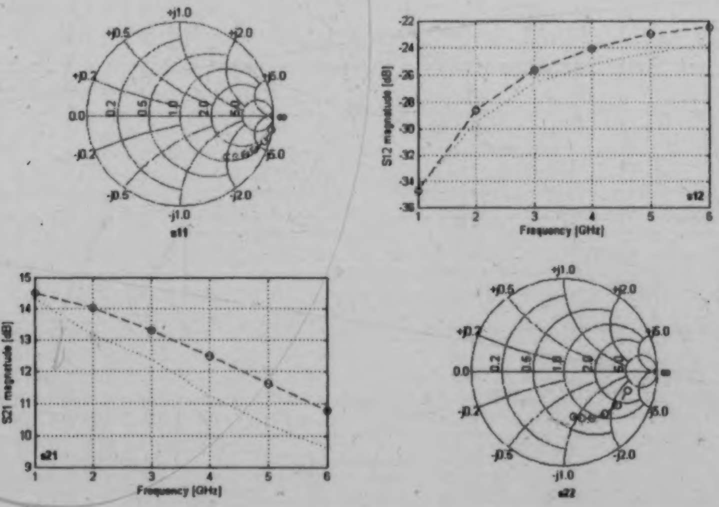


Figure 3-5: Comparison of measured (o) and simulated using lumped elements (*) S-parameters for an NMOS device; W = 120 μm, L = 0.18 μm.

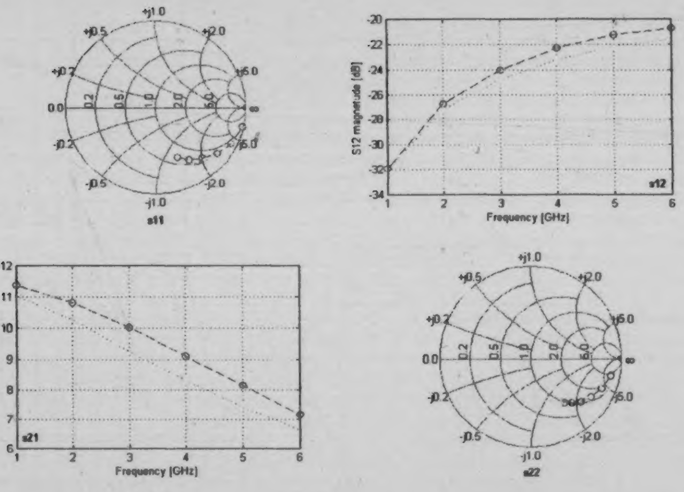


Figure 3-6: Comparison of measured (o) and simulated using lumped elements (*) S-parameters for an NMOS device; *W* = 120 μm, *L* = 0.36 μm.

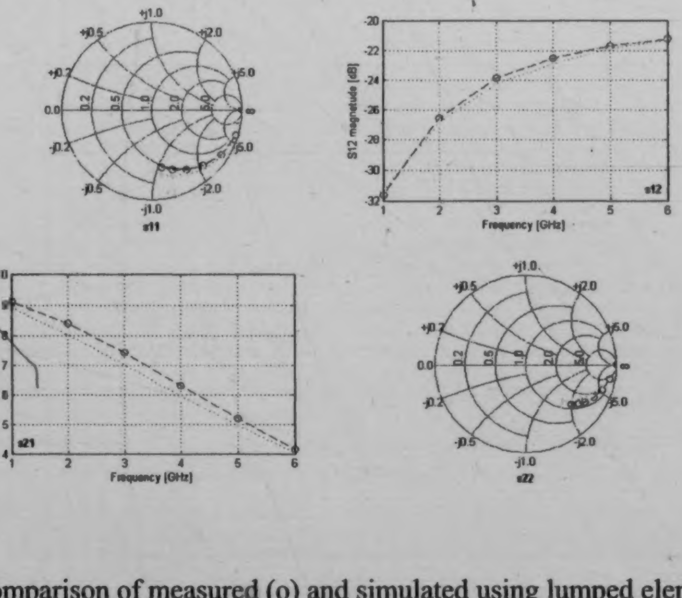


Figure 3-7: Comparison of measured (o) and simulated using lumped elements (*) S-parameters for an NMOS device; *W* = 120 μm, *L* = 0.54 μm.

The procedure described in section 3.2.3, can be repeated to determine the small-signal model at multibias points. Figure 3-8 depicts the measured parameters of the small-signal MOSFET model plotted as a function of the gate and drain bias at 3 GHz. The transconductance g_m is shown in Figure 3-8.a. The transconductance decreases with the reduction of V_{gs} in accordance with theoretical expectations. The dependence of g_m on V_{ds} is minimal since measurements are done on a MOSFET operating in the saturation region. The output conductance g_{ds} shown in Figure 3-8.b is highly dependent on V_{gs} as expected from the characteristics of the drain current versus the drain source voltage of the MOSFET. The variation trends of C_{gs} versus V_{gs} and V_{ds} are similar to the variations of the transconductance shown in Figure 3-8.a. The value of C_{gs} almost doubles as V_{gs} changes from 0.5 V to 1.8 V.

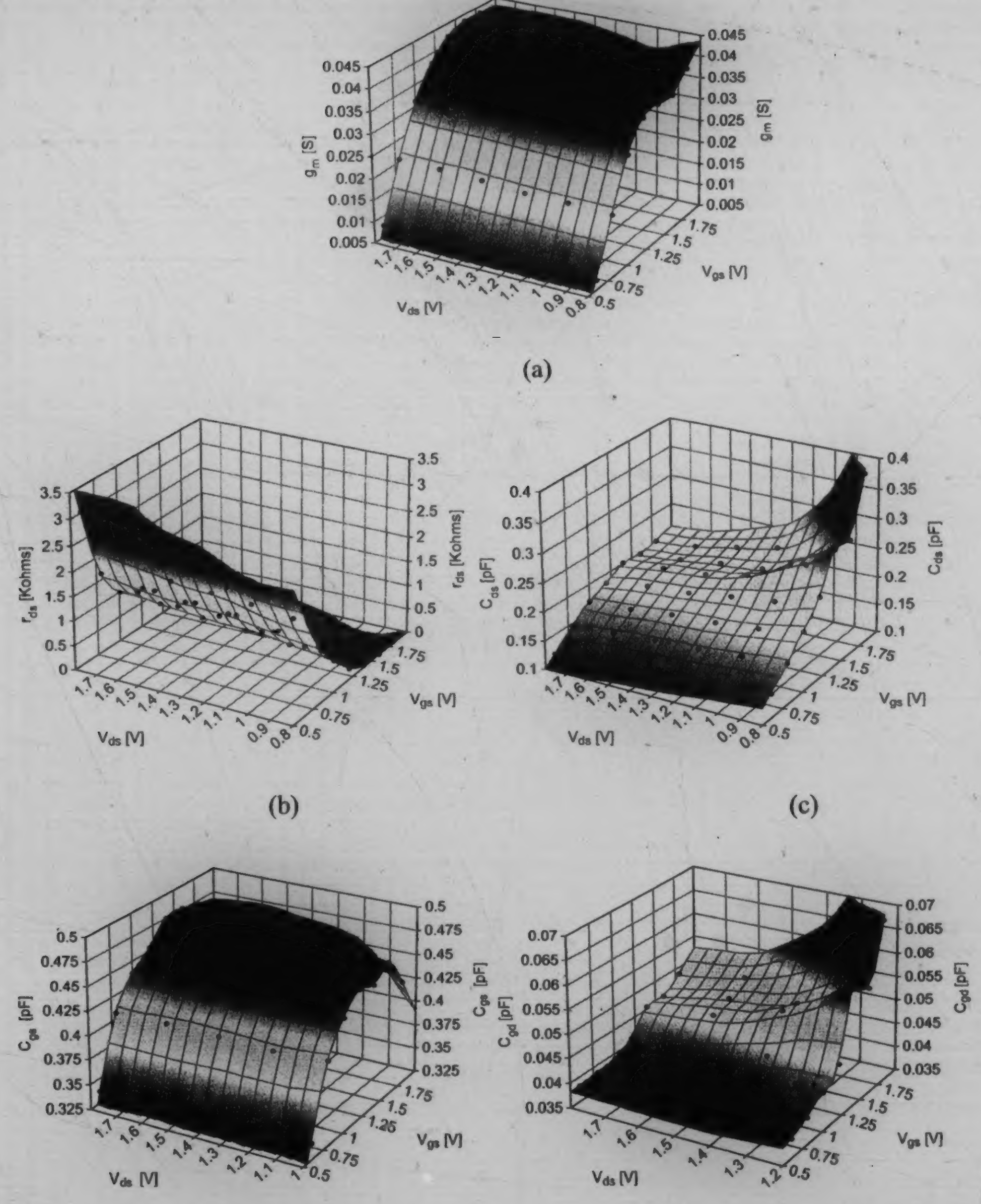


Figure 3-8: Measured small-signal parameters of an N type MOSFET with $W = 120$ μm and $L = 0.54$ μm versus V_{gs} and V_{ds}.

3.3 Drain current noise measurement

For MOSFETs operating at high frequencies, the main noise source is the drain current noise originating from the random motion of free carriers in the channel formed between source and drain. For long channel MOSFET devices, the model proposed by Van der Ziel predicts the channel noise successfully [29]. For short channel devices, values of observed channel noise were higher than predicted by the Van der Ziel model [31]. Several models of channel thermal noise of MOSFET devices operating at radio frequency have been proposed recently [31] for the channel thermal noise of MOSFET devices operating at radio frequencies. Models of channel thermal noise compared in this paper are suitable for circuit analysis, and are given by [17]:

$$S_{id} = \frac{8}{3} kT g_m, \tag{3.12}$$

$$S_{id} = \frac{8}{3} kT \left(g_m + g_{ds} \right), \tag{3.13}$$

and

$$S_{id} = \frac{8}{3} kT \left(g_m + g_{ds} + g_{mb} \right), \tag{3.14}$$

where K is the Boltzmann constant, T is the absolute temperature in Kelvin degrees, g_m is the transconductance, g_{ds} is the drain source conductance, and g_{mb} is the body transconductance. In addition, we evaluate the model suggested by Deen *et al.* [31] which describes the thermal channel noise in terms of voltages and currents:

$$S_{id} = 4kT \frac{4V_{GT}^2 + V_d^2 + V_d V_{GT}}{3V_{GT}^2 \left(V_{GT} - V_d \right)} \alpha I_D. \tag{3.15}$$

Here, $V_{GT} = V_{gs} - V_{th}$, α is a coefficient accounting for bulk charge effects (a typical value is around 1.2 [31], and V_d is given by:

$$V_d = \frac{I_D}{WC_{ox}v_{sat}}, \tag{3.16}$$

where I_D is the drain bias current, W is the device width, and v_{sat} is the saturation velocity.

Several steps are required to extract the MOSFET drain current noise [13]; they include measuring the S-parameters of test devices, extracting the parameters of the MOSFET high frequency small-signal model, and measuring the MOSFET noise parameters. In addition, many parasitics are introduced by the probe pads and the metallization that surround the device under test (DUT). In order to obtain characteristics of the intrinsic transistor, effects of these parasitics must be de-embedded from the measured S and noise parameters [13].

3.3.1 Noise parameter de-embedding

The probe pads and parasitics surrounding the device can affect the noise figure measurements of an on-wafer device [13], [45]. As explained in Chapter 2, the pads capacitively couple through the oxide layer to the substrate. The substrate underneath the pad behaves like a resistor, a source of noise. In addition, extrinsic elements surrounding the MOSFET generate thermal noise that degrades the noise figure. Methods to split the contribution of the pads and the parasitics surrounding the intrinsic FET begin with the admittance noise correlation matrix given by:

$$[C_A] = 2kT_0 \begin{pmatrix} R_n & \frac{F_{\min} - 1}{2} - R_n Y_{opt}^* \\ \frac{F_{\min} - 1}{2} - R_n Y_{opt} & R_n \left| Y_{opt} \right|^2 \end{pmatrix}, \tag{3.17}$$

where k is Boltzmann's constant, T_0 is the ambient temperature, R_n, F_{min}, and Y_{opt} are the MOSFET noise parameters. For a passive device the correlation matrix can be given by:

$$[C_Y] = 2kT.\mathrm{Re}[Y], \tag{3.18}$$

where C_Y is the noise correlation matrix and Y is the admittance two port parameters of the passive device. The next step is to convert the correlation matrix into ABCD noise matrices. This is done through multiplying C_Y by a transformation matrix T:

$$[C_A] = [T][C_Y][T]^+, \tag{3.19}$$

Here the transformation matrix T and its transpose T^+ are:

$$\begin{gathered} [T] = \begin{pmatrix} 0 & a_{12} \\ 1 & a_{22} \end{pmatrix} \\ [T]^+ = \begin{pmatrix} 0 & 1 \\ a_{12} & a_{22} \end{pmatrix} \end{gathered}, \tag{3.20}$$

where a_{12} and a_{22} are elements of the two-port ABCD or chain matrix defined as:

$$[A_{meas}] = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix}. \tag{3.21}$$

The noise correlation matrix for the intrinsic FET is then found using

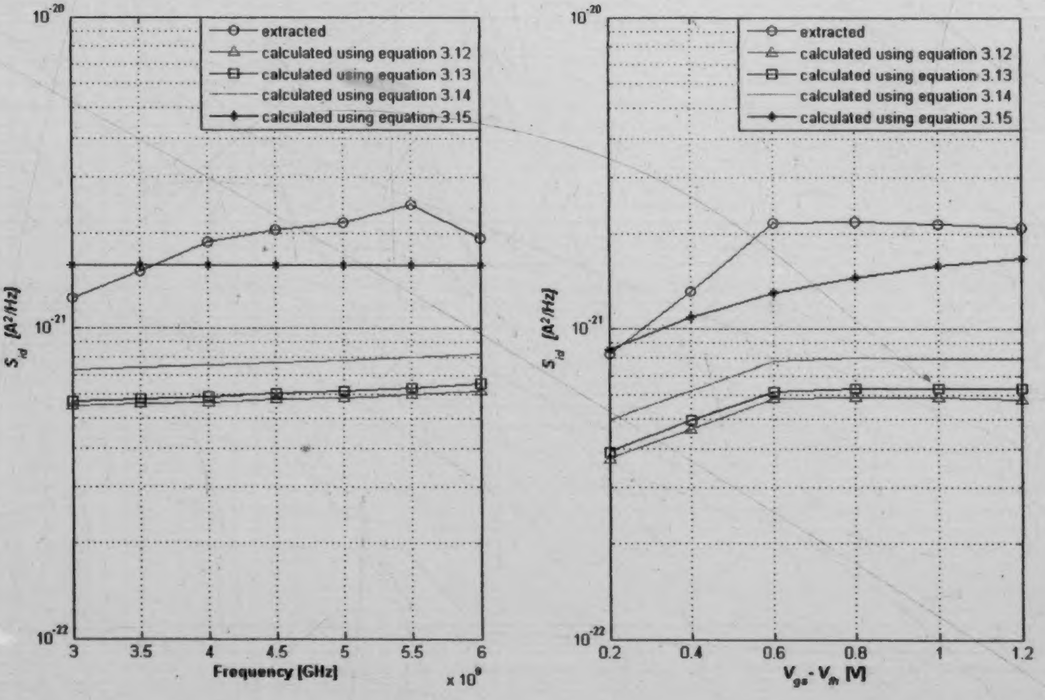
$$[C_{A,FET}] = [A_{gate}]^{-1} \left([C_{A,tot}] - [C_{A,gate}] \right) [A_{gate}]^{+^{-1}} - A_{FET} C_{A,drain} A_{FET}^+ \tag{3.22}$$

The matrix $C_{A,tot}$ is the measured noise performance of the FET embedded in pads and interconnects. $C_{A,gate}$ and $C_{A,drain}$ are the correlation matrices for the gate and drain parasitics. The drain current noise can then be calculated using:

$$S_{id} = 4kT_0R_n|Y_{21}|^2 \, . \tag{3.23}$$

3.3.2 Measurement results

The extracted channel noise (from measurements) for a representative NMOSFET (0.36 μm gate length) is shown in Figure 3-9.a. It is approximately $0.2*10^{-20}$ [A^2/Hz] over a frequency range of 3–6 GHz with a gate overdrive voltage ($V_{gs} - V_{th}$) of 0.6 V and a V_{ds} of 1.8 V. Channel thermal noise as a function of gate overdrive voltage is shown in Figure 3-9.b.



(a) (b)

Figure 3-9: Extracted and calculated drain current noise (a) versus frequency; and (b) versus gate overdrive voltage measured at 5 GHz; V_{ds} = 1.8 V, W/L = 120 μm/0.36μm.

The extracted channel thermal noise was approximately $0.7*10^{-20}$ and 10^{-21} [A^2/Hz] for the 0.18 μm and 0.54 μm gate length MOSFETs, over a frequency range of 3–6 GHz with a gate overdrive voltage ($V_{gs} - V_{th}$) of 0.6 V and a V_{ds} of 1.8 V. Extracted results from measurements and calculated results for the NMOSFETs with W/L 120 μm/0.18 μm and 120 μm/0.54 μm are compared in Table 3-1. Comparisons were done at 5 GHz with a gate overdrive voltage of 0.6 V. The simple model of drain current noise of short channel devices operating at RF frequencies presented by Deen *et al.* [31] provided the best match between extracted and calculated thermal noise over a frequency range of 3 GHz to 6 GHz and an overdrive voltage range of 0.2 V to 1.2 V.

Table 3-1: Comparison between extracted and calculated drain current noise models.

	NMOSFET 120 μm/0.18 μm S_{id}(A^2/Hz)	NMOSFET 120 μm/0.54 μm S_{id}(A^2/Hz)
Extracted from measurements	7.4e-21	9.8e-22
Calculated using equation (3.12)	0.82e-21	3.44e-22
Calculated using equation (3.13)	0.88e-21	3.63e-22
Calculated using equation (3.14)	1.17e-21	4.6e-22
Calculated using equation (3.15)	5.25e-21	7.9e-22

3.4 Conclusion

Two steps are needed to extract the drain current noise a of MOSFET The first step includes extracting the RF small signal equivalent circuit of the MOSFET. The second step includes noise parameters deembeding and extraction of the drain current noise.

A method to extract the MOSFET RF small-signal parameters from S-parameter measurements is presented. Extracted MOSFET RF small-signal-models were validated by comparing measured and extracted S-parameters of MOSFET devices with widths of 0.18 µm, 0.36 µm, and 0.54 µm. A comparison among several drain current noise models suitable for hand analysis indicates that the model developed by Deen *et al.* provides the closest agreement between modeled and measured results.

Chapter 4

Oscillators in CMOS Technology

4.1 Introduction

In many RF and wireless systems, phase noise is a key measure of oscillators performance. One of the benefits of phase noise reduction is an increase in the number of users of a fixed bandwidth wireless system, which translates to profits for service providers. Despite extensive efforts by researchers over several decades, phase noise of electrical oscillators is still an active research area. A justification for the continuous research activity can be found in Rohde's statement [59], *"In designing VCOs, minimizing phase noise is the prime task. This has been accomplished using empirical rules or numerical optimization, which are often held as trade secrets by many manufacturers."* Over a time span of several decades, contributions to phase noise theories have been made by different groups of researchers and different approaches have been taken to model phase noise in oscillators [59]–[74]. In 1966, Leeson provided an insightful though qualitative approach to LC oscillator phase noise mechanisms [60]. A CAD oriented approach, was taken by [61], [62], with little benefit to circuit designers. An approach more oriented to circuit design was suggested by [62]–[75]. A method to classify the various contributions to phase noise theories can be decided according to the device type used, discrete or integrated. One researcher group studied phase noise using oscillators built with discrete devices, while other groups researched phase noise using integrated devices. Each group of researchers took a different approach to phase noise analysis. Also, each group used different semiconductor technologies and studied phase noise over different frequency bands. In discrete design, usually oscillators are built using only one active element. This constraint is needed in order to minimize cost and also to reduce interconnection complexity. However, these constraints are of no importance in IC design due to the reduced cost of active elements and the ease of interconnection fabrication. In addition, IC designers have the freedom to tailor the active device width but have constraints of low voltage and low power designs.

In phase noise theories presented by discrete design researchers, some researchers focused on achieving an optimum match between the active element and the resonator in order to reduce phase noise. For example, in low noise amplifier (LNA) design, the input matching to the active element directly impacts the amplifier noise figure. Leindenmeir [63] realized that a similar matching technique could be applied to oscillators in order to reduce phase noise. Everard [65] emphasized the effect on phase noise of coupling between a single active element and the resonator. Llopis and Cibiel presented a theory of correlation between an active element low frequency noise and oscillator phase noise [67]. In [68], phase noise theories of discrete devices were extended to include a method of matching to a device operated in a large signal regime.

Phase noise theories provided by IC designers include [71]–[75]. However, concepts such as optimum coupling and large signal matching developed by discrete oscillator designers were ignored in other phase noise theories developed by IC designers. For example, Hajimiri and Lee [71] suggested minimizing an impulse sensitivity function in order to reduce phase noise while ignoring the effects of the mismatch between the active device and the resonator. To bridge the gap between discrete and integrated phase noise theories, Cordeau *et al.* [75] suggested biasing the oscillator active device as a class C amplifier while optimizing resonator matching. In [76], phase noise was improved using a voltage dividing and bias-level shifting technique.

In the first section of this chapter, a brief review of the main phase noise theories will be presented. An emphasis will be placed on the conditions of application of each theory (assumptions of the theory, frequency of operation, technology used, oscillator type, etc.). We will restrict the review to the design oriented theories.

4.2 Definition of phase noise

IEEE Standard 1139-1999 covers methods of describing the random instabilities of importance to frequency and time metrology [77]. Quantities defined in IEEE Standard 1139-1999 include frequency, amplitude, and phase instabilities; and the spectral density of frequency, amplitude, and phase fluctuations. In this standard, the instantaneous output voltage of a precision oscillator can be expressed by:

$$V(t) = (V_0 + \varepsilon(t))\sin(2\pi\nu_0 t + \phi(t)), \tag{4.1}$$

where V_o is the nominal peak amplitude of the oscillator, $\varepsilon(t)$ is the deviation from nominal amplitude, ν_o is the nominal frequency, and $\phi(t)$ is the phase deviation from the nominal phase $2\pi\nu_0 t$. IEEE Standard 1139-1999 describes frequency instabilities that result from fluctuations of the oscillation period. Fluctuations in phase result in instability of the zero crossing of the signal. Fluctuations in the peak value of the signal result in amplitude fluctuations. The amplitude-limiting mechanism of the oscillator usually damps amplitude fluctuations. However, no mechanism exists in the oscillator to damp phase fluctuations. A limit cycle can be used to describe the stability of oscillators [78]. Due to the presence of an amplitude limiting mechanism, for stable oscillators, radial perturbations remain small and the oscillator always return to the limit cycle. On the other hand, no restoring force exists in the oscillator to control fluctuations along the limit cycle. Consequently, the oscillator phase undergoes a random walk or diffusive motion [78]. Ham and Hajimiri [79], and Magierowski [80] showed that the associated constant of diffusion is the parameter that characterizes phase noise.

In the frequency domain, phase instabilities can be characterized by the spectral density of phase fluctuations $S_\phi(f)$, given by [77]:

$$S_\phi(f) = \phi^2(f)\frac{1}{BW}, \tag{4.2}$$

where BW is the measurement system bandwidth in Hz. The units of $S_\phi(f)$ are rad^2/Hz. A commonly used measure of phase noise is $\mathcal{L}(f)$ which is the ratio of the power in one sideband due to phase modulation by noise (for a 1 Hz bandwidth) to the total signal power (carrier plus sideband). Usually $\mathcal{L}(f)$ is expressed in decibels (dB) as 10 log$\mathcal{L}(f)$, and its units are dB below the carrier in 1 Hz bandwidth, generally abbreviated as dBc/Hz. $\mathcal{L}(f)$ can be defined as one half of the double-side band spectral density of the phase fluctuations $S_\phi(f)$ [77]:

$$\mathcal{L}(f) \equiv \frac{S_\phi(f)}{2}. \tag{4.3}$$

It should be noted that $\mathcal{L}(f)$ is measured at a specific frequency offset from the carrier. $\mathcal{L}(f)$ does not provide information about phase noise at other offset frequencies except when a slope of phase noise curve versus frequency is provided. It is therefore preferable to make a plot of 10 log$\mathcal{L}(f)$ as a function of carrier offset frequency, the latter on a logarithmic axis.

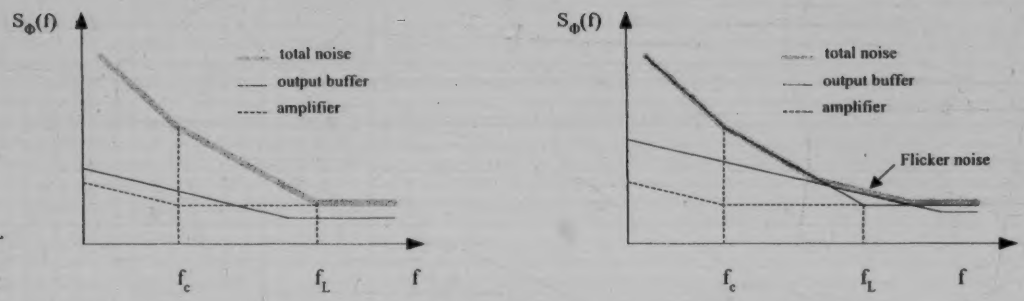
The phase noise spectrum can be divided into three regions depending upon the offset from the carrier. The first region is closest to the carrier and is believed by many authors to be caused by flicker noise upconversion [81]. The second region is due to thermal noise conversion to near carrier noise [82]. The third region corresponds to the oscillator thermal noise floor in addition to converted thermal noise from harmonic frequencies [71]. According to Leeson [60], the frequency at which the noise flattens out is equal to half the resonator bandwidth given by:

$$\omega_L = \omega_0/2Q, \tag{4.4}$$

where ω_0 is the resonance frequency and Q is the resonator quality factor. However, as will be shown in section 4.4.4, Hajimiri and Lee refuted this assumption [71]. An output buffer is usually used at the output of an oscillator to prevent the change of the oscillation frequency with the oscillator load change and to reduce the power needed for oscillator startup as will be shown in section 4.5.1. The effect of the output buffer on the phase noise spectrum will be discussed in the next section.

4.2.1 Effects of buffers on phase noise

Building on the insight gained from Leeson's theory [60], Rubiola and Giordano [83] and Rubiola [84] investigated changes that a buffer can introduce in an oscillator spectrum. These changes depend on the relation of the corner frequency (f_c) in the buffer amplifier flicker noise spectrum to the Leeson corner frequency (f_L) [83], [84]. Two of the important cases discussed by Rubiola [83] are shown in Figure 4-1. The combined spectrum of the oscillator phase noise, oscillator amplifier flicker noise, and the buffer amplifier phase noise is shown in Figure 4-1. In Figure 4-1.a the buffer amplifier and the oscillator amplifiers have similar flicker characteristics and ($f_L > f_c$). The insertion of the output buffer does not affect the oscillator spectrum. In Figure 4-1.b the phase flickering of the buffer adds to the phase noise of the oscillator. As a consequence, the corner point f_L is turned toward lower frequencies and a region with a slope of 1/f appears in the oscillator spectrum.



(a) (b)

Figure 4-1: (a) Buffer amplifier flicker noise does not affect the oscillator phase noise spectrum; (b) Buffer amplifier flicker noise alters the oscillator phase noise spectrum [84].

The use of an active stage as buffer might deteriorate some of the performance parameters of the oscillator. For example, the signal swing over the resonator node, that is driving the active stage buffer, might need to be reduced in order to not push the buffer stage into compression as the resulting harmonics from the compressed buffer stage might corrupt the oscillator spectrum. These harmonics could be coupled to other circuits through the silicon substrate. In addition, these harmonics might be radiated if they reach the antenna through the reverse isolation of the front end. Another drawback of reducing the signal swing over the tank node is the increase in phase noise as shown by [60], [71]. Also, the added parasitic capacitance of the active buffer stage might slightly reduce the tuning range of a voltage-controlled oscillator.

Most buffers reported in the literature for CMOS oscillators were designed for narrow band, low oscillator power applications that operate at low GHz frequencies (1 GHz to 5

GHz). With improvement in the cutoff frequency (f_t) of CMOS technology, wide band CMOS oscillators and oscillators operating at 20 GHz and 100 GHz were recently reported in the literature [85], [86]. Also, applications requiring high oscillator power were reported for oscillators designed in SiGe technology [87]. The new design requirements of high operating frequency, wide tuning bandwidth, high output power, and low power operation, pose several challenges for the buffer stage design. In order to meet the design requirements of newly emerging applications, the buffer stage should remain stable, provide good isolation, provide maximum output power to the load, and maintain high linearity over the operating frequency band. Buffer stage topologies reported in the literature depend on the application. In a 50 ohms environment, because of its low output impedance, the common drain configuration was widely used to drive test equipment without degrading the LC tank quality factor [88]. The conventional common drain stage and the use of transformers to extract the oscillator signal were compared in [88]. An oscillator with a buffer transformer showed higher output power, better power efficiency, and better harmonic suppression compared to an oscillator buffered by a common drain stage [88]. The transformer buffer, however, occupies a larger chip area, reduces tuning range, and is limited to narrow band operation. Various amplifier configurations were used as buffers in order to increase the oscillator signal swing [86]–[88]. To reduce power consumption, Steyaert *et al.* [89] eliminated the use of buffers by careful circuit design.

4.3 Comments on phase noise models

In addition to differences between the several phase noise theories presented in the previous sections, researchers differed in several other aspects of the proposed phase noise models. Llopis [90] indicated the absence of a standard method to mathematical modeling of a noisy nonlinear system. For example, in almost all phase noise theories, the noisy oscillator was modeled as an active block excited by external noise sources. However, the choices of active block mathematical model and noise sources model varied widely among researchers. A group of researchers represented the oscillator as a linear time-invariant system [60]. This mathematical modeling of the oscillator was adopted by [91]; the authors stated: *"Another way to view this signal growth and the resulting steady state oscillation is to consider the oscillator as a multitude of amplifier resonator stages."* Also, in [92] the authors state, *"An oscillator is a narrow band amplifier of noise"* and *" With the help of stochastic signal theory we can show that a noise signal filtered through a very narrow band is nearly sinusoidal and the degree of coherence increases as the bandwidth becomes smaller. On the other hand, we can learn from this that an oscillator can be never be totally noise free."* To overcome differences between the actual phase noise spectrum and the phase noise spectrum predicted by Leeson [60], Hajimiri and Lee [71] modeled the oscillator as a linear time-varying block. Magierowski and Zukotynski [73] modeled the oscillator as a nonlinear block.

The controversy between researchers is even greater in modeling noise sources. Some researchers used the two-port small-signal noise model presented in chapter two of this thesis [63]. Other researchers excited a linear block representing the oscillator by a thermal noise source representing the noise from active and passive elements in the oscillator circuits. In the theory developed by Hajimiri and Lee [71], a time-varying linear block representing the oscillator was excited by a cyclostationary noise source and phase noise appeared due to the upconversion of flicker noise and due to thermal noise as will be shown in section 4.4.4. Another important parameter in phase noise modeling is the physical location of the noise source compared to the oscillator's modeling block.

O. Llopis and G. Cibel [67] discussed noise models in linear circuits compared to noise models of nonlinear circuits stating: "*In linear noise modeling it is not essential to physically locate a noise source in the transistor model. An equivalent noise sources approach is generally used, with two intrinsic noise sources and their correlation factor. On the contrary, in nonlinear circuits, the location of a noise source versus a nonlinear element is essential. If this noise source modulates a nonlinear element, it will be transposed to higher frequencies and generate phase noise. If it is at the transistor output, it can not modulate the main nonlinear elements in the device and has a very weak effect on the phase noise.*"

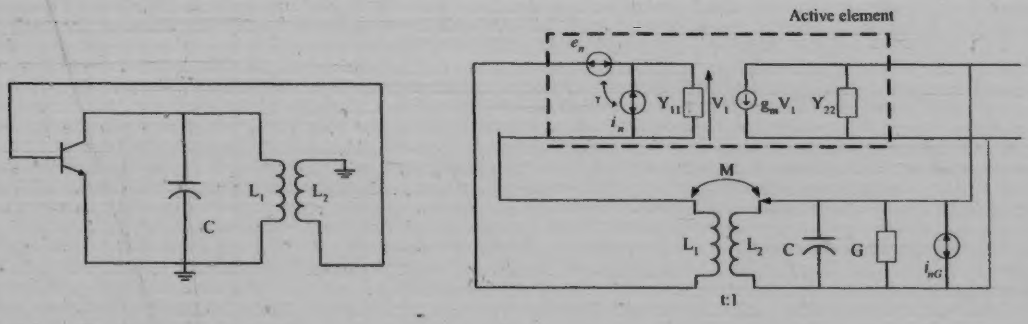
4.4 Main phase noise models

4.4.1 The Braun and Lindenmeier model

A unique aspect of the Braun and Lindenmeier theory is the use of small-signal noise matching in order to reduce oscillator phase noise [63], [64]. In low noise amplifier design, the source impedance (50 ohms) is transformed through a matching circuit to another impedance Γ_{opt} (optimum noise resistance) in order to minimize the amplifier noise factor as was shown by Lee [8] and Gonzalez [27]. Braun and Lindenmeier [63], [64] demonstrated that a similar noise-minimization technique could be used to reduce the noise contributed by the active stage to the oscillator phase noise. As the feedback circuit in an oscillator can be modeled using a transformer, the impedance seen at the input of the amplifier is then the amplifier output impedance divided by the squared transformer turns ratio. By modifying the transformer turns ratio, impedance matching at the input port of the active device for minimum noise figure can be achieved.

In Braun and Lindenmeier's [63] theory, a small signal for the transistor is assumed and the noisy two-port amplifier is represented by a noiseless two-port with two correlated noise current and noise voltage sources v_n and i_n, respectively. The correlation is represented by the complex correlation coefficient γ. Flicker noise upconversion is ignored in this theory. A good agreement was found between theory and measurements done on a 150 MHz oscillator. The oscillator topology used by Braun and Leindenmeier [63] and the equivalent circuit of the oscillator are shown in Figure 4-2. G represents the tank losses, L and C

represent the tank circuit inductance and capacitance, respectively. The noise current i_{nG} consists of the thermal noise of the conductance G, t is the primary to secondary transformer ratio.



(a)

(b)

Figure 4-2: (a) Oscillator AC equivalent circuit; (b) Noise equivalent circuit [63].

The carrier to noise ratio at the output of the oscillator can be given by:

$$a_{Fm} = 10.\log\left[\frac{BKT.f_0^2}{p}\cdot\frac{G_e}{G}\cdot\frac{1}{Q_0}\cdot\frac{1}{\Delta f^2}\right], \tag{4.5}$$

where P is the oscillator power, K is Boltzmann's constant, B is the noise measurement bandwidth, Δf is a frequency offset from the carrier, and Q_0 is the resonant circuit quality factor determined by the conductance G. G_e is given by:

$$G_e = \frac{\overline{i_{nG}^2} + \overline{i_{nT}^2}}{4.KT.B}, \tag{4.6}$$

where i_{nT} represents the active element noise sources transformed into a single noise current source parallel to the tank. The aim of the theory is to find the minimum ratio G_e/G necessary to minimize equation (4.5). Braun and Lindenmeier [63] demonstrated that the minimum ratio of G_e/G is achieved when the conductance G_{tot} is transformed via the feedback circuit into the optimum source admittance Y_{opt} at the input of the transistor:

$$\left(\frac{G_e}{G}\right)_{\min} = 1 + \frac{F_{T\min}}{\left(\gamma_R + \sqrt{1-\gamma_I^2}\right)} \cdot \frac{G_{tot}}{G}, \tag{4.7}$$

where γ_R and γ_I are the real and imaginary parts of the complex correlation coefficient shown in Figure 4-2. F_{Tmin} represents the minimum noise figure of the noise matched active element. G_{tot} can be given by:

$$G_{tot} = G + \mathrm{Re}\{Y_{22}\}. \tag{4.8}$$

where $\mathrm{Re}\{Y_{22}\}$ is the real part of the admittance parameter Y_{22}.

4.4.1.1 Results of Braun and Lindenmeier's phase noise theory

According to Braun and Lindenmeier [63], the following recommendations can be applied in order to design an oscillator with low phase noise:

1. Choose a transistor with small noise figure F_{Tmin} and small output conductance.

2. Maximize the oscillator output power.

3. Meet an impedance condition at the input of the active element, which can be reached by optimization of the oscillator feedback network.

4. Choose a resonator with high quality factor Q_0.

4.4.2 Everard phase noise model

Everard [65] and Everard and Page-Jones [66] presented a theory for low noise oscillator design to describe the effects of the amplifier noise figure (*F*), the voltage gain of the amplifier (*G*), the unloaded quality factor (Q_0), and the loaded quality factor (Q_L) on phase noise. The theory was verified experimentally for oscillators built using different semiconductor technologies in the frequency range from 150 MHz up to 7 GHz. A linear model was used for the oscillator. Flicker noise effects on oscillator phase noise performance were described qualitatively. Suggested oscillator topologies to reduce phase noise were presented in [65], [66].

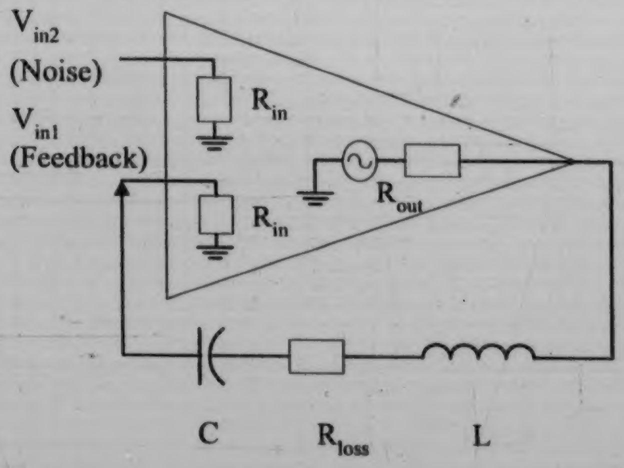


Figure 4-3: Everard equivalent circuit model of an oscillator [65].

The oscillator equivalent circuit shown in Figure 4-3 was used to calculate phase noise. The Everard model of an oscillator consists of an amplifier with two inputs with equal impedance. The first input is driven by the feedback resonator voltage (V_{in1}); the second input is driven by the circuit noise voltage (V_{in2}). The output impedance is given by R_{out}. A capacitor C, an inductor L, and a loss resistance R_{loss} model the feedback resonator. The circuit configuration is similar to an operational amplifier with feedback circuit, therefore the voltage transfer characteristic can be derived in a similar way. The phase noise at an offset frequency f_0 from the carrier can be given by:

$$\mathcal{L}_{FM} = A.\frac{FKT}{8.(Q_0)^2 (Q_L/Q_0)^2 (1-Q_L/Q_0)^N \, P}\left(\frac{f_0}{\Delta f}\right)^2, \tag{4.9}$$

where A and P are constants that depend on the input and output impedance of the amplifier shown in Figure 4-3, F is the operating noise figure, K is Boltzmann's constant, T is the operating temperature in degrees Kelvin, Q_L is the loaded quality factor, Q_0 is the resonator unloaded quality factor, and f_0 is the operating frequency. If equation (4.9) is differentiated with respect to Q_l/Q_0, a minimum value of phase noise can be obtained at $Q_l/Q_0 = 2/3$. If the oscillator is operating with the optimum value of Q_l/Q_0, then the equation of phase noise simplifies to:

$$L_{FM} = A.\frac{27 \cdot FKT}{32.(Q_0)^2 P_{RF}}\left(\frac{f_0}{\Delta f}\right)^2, \tag{4.10}$$

where P_{RF} is the total RF power. The theory described above is valid when thermal noise is the dominant noise source. The effect of flicker noise can be incorporated into this theory by shaping part of the input noise with a 1/f characteristic. Several circuits were described in [2] for transposed flicker noise reduction.

4.4.2.1 Results of Everard's theory

1- The resonator should have a high-unloaded quality factor.

2- The loop amplifier should have a low small-signal noise figure.

3- Resonator coupling should be set to achieve the ratio between loaded and unloaded quality factor = (1/2) or (1/3).

4- An oscillator configuration producing the lowest transposed flicker noise should be implemented.

4.4.3 Llopis and Cibiel's theory

Llopis and Cibiel [67] predicted that the noise characteristics of the oscillator's components as measured in an open-loop (residual phase noise) configuration have a direct bearing on the closed loop phase noise of the oscillator. The study of the oscillator components in an open-loop configuration has several advantages over a closed loop analysis of the oscillator. The first advantage is in the simulation domain: the analysis of a driven circuit (an amplifier) is easier and quicker than the analysis of an autonomous circuit. The second advantage is in the experimental domain: the noise performance of an amplifier can be measured in a very precise way. The open-loop phase noise approach (or residual phase noise approach) has revealed many interesting points that can be used for oscillator phase noise minimization. The oscillator block diagram shown in [67] is used to study the sources of phase noise in an oscillator. The block diagram represents an active element and a tuned circuit in a feedback configuration.

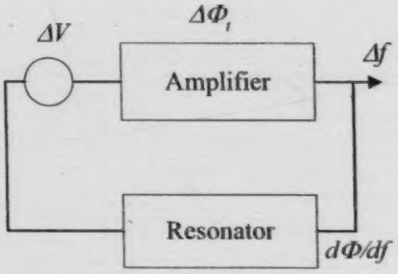


Figure 4-4: Simplified feedback oscillator model [67].

Three sources of noise are represented on the simplified feedback oscillator model shown in Figure 4-4. ΔV represents the equivalent low frequency noise at the input of the oscillator, $\Delta\phi_t$ is the residual phase noise of the transistor in an open-loop configuration, and Δf represents frequency fluctuations around the carrier. The goal of the current theory is to determine the correlation between Δf, $\Delta\phi$, and ΔV. The active device phase fluctuations in an oscillator loop are directly converted into frequency fluctuations according to [67]:

$$S_{\Delta f} = \left[\frac{f_0}{2Q_L}\right]^2 S_\phi, \qquad (4.11)$$

where $S_{\Delta f}$ is the oscillator frequency fluctuations spectral density (in $\mathrm{Hz}^2/\mathrm{Hz}$), S_ϕ is the amplifier phase noise spectral density (in $\mathrm{rad}^2/\mathrm{Hz}$), f_0 is the oscillator frequency, and Q_L is the oscillator loaded quality factor. Therefore, investigations of Δf can be replaced by investigations of $\Delta\phi$. The three sources of noise (Δf, $\Delta\phi$, and ΔV) can be correlated by the following simplified process: ΔV generates fluctuations of certain resistive and capacitive elements in the active device resulting in phase fluctuations in the device when the active device is used as an amplifier (open-loop configuration). When the amplifier is used in a closed loop, the condition of oscillation requirements needed for oscillation build-up impose a total phase of 2nπ around the loop. The phase fluctuations caused by the active device have to be compensated by fluctuations in another circuit parameter in order to satisfy the phase conditions needed for oscillation build-up. If we assume that the amplitude fluctuations are either weak or have been removed by the closed-loop amplitude limiter, then the frequency in the loop will be the only fluctuating parameter [67]. It can be shown that the oscillator phase noise can be given by [68]:

$$\mathcal{L}_{osc}(f_m) = 20\log\left(\frac{f_0 \cdot \Delta\phi_l}{2\sqrt{2} \cdot Q_L \cdot f_m}\right), \tag{4.12}$$

where $L_{osc}(f_m)$ is the oscillator phase noise at an offset frequency f_m from the carrier f_0, $\Delta\phi$ is the residual phase fluctuation of the active device, and Q_L is the oscillator loaded quality factor. The main addition of Llopis and Cibiel's [67] theory is the use of residual phase noise measurement as a criterion for the selection of transistor used as an active element in the oscillator feedback loop.

4.4.4 The Hajimiri phase noise model

Hajimiri and Lee [71] were the first to point out the limitations of the phase noise theories developed using a linear oscillator model. Hajimiri and Lee modeled the oscillator as a linear time-varying system driven by a cyclostationary noise source. The main outcome of the theory is the proposal of a new function that measures the sensitivity of the oscillator to an applied impulse. The proposed function was called an impulse sensitivity function (ISF) and it measures the sensitivity of an oscillator to a current impulse injected in the resonator at a particular moment. Using Spice simulation, Hajimiri and Lee concluded that injecting the noise current into the resonator at a waveform peak produces a change in amplitude. This amplitude change is attenuated by the oscillator's amplitude control mechanism. Injecting the current impulse at a zero crossing causes a phase disturbance. Unlike amplitude disturbance, no mechanism exists in the oscillator to attenuate the phase disturbance. The impulse response of the resonator due to injection of the noise current pulse can be given by:

$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_0 \tau)}{q_{\max}} u(t-\tau), \tag{4.13}$$

where $u(t)$ is the unit step function, τ is the time when the impulse is injected, and q_{max} is the maximum value of the injected charge into the capacitor. The function $\Gamma(x)$ is the time-varying "proportionality factor." It is called the *impulse sensitivity function* (ISF), since it determines the sensitivity of the oscillator to an impulsive input. The output excess phase $\phi(t)$ can be calculated using:

$$\phi(t) = \int_{-\infty}^{\infty} h_{\phi}(t,\tau) i(\tau) d\tau = \frac{1}{q_{\max}} \int_{-\infty}^{t} \Gamma(\omega_0 \tau) i(\tau) d\tau \,. \tag{4.14}$$

Since the ISF is a periodic function at frequency ω_0, only noise close to DC, ω_0, and its harmonics will result in a nonzero excess phase as seen from equation (4.14) [93]. Noise from all other frequencies will average-out over time. Using the Fourier series, the ISF can be expanded as:

$$\Gamma(\omega_0\tau) = c_0 + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau + \theta_n), \tag{4.15}$$

where the coefficients c_n are real-valued, and θ_n is the phase of the nth harmonic. Substituting equation (4.15) in equation (4.14) gives:

$$\phi(t) = \frac{1}{q_{\max}}\left[c_0 \int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau)\cos(n\omega_0\tau)d\tau\right]. \tag{4.16}$$

Equation (4.16) identifies individual contributions to the total $\phi(t)$ for an arbitrary input current $i(t)$ injected into any circuit node in terms of the various Fourier coefficients of the ISF. The phase noise spectrum in the $1/f^2$ region may be expressed as:

$$\mathcal{L}(\Delta\omega) = 10.\log\left[\frac{\frac{\overline{i_n^2}}{\Delta f}\Gamma_{rms}^2}{2q_{\max}^2\Delta\omega^2}\right]. \tag{4.17}$$

Where Γ_{rms} is the root mean squared value (rms) value of the ISF, q_{max} is the maximum charge on the tank capacitance, and i_n is the noise current source injected in the tank. Phase noise due to flicker noise can be given by:

$$\mathcal{L}(\Delta\omega) = 10.\log\left[\frac{c_0^2}{q_{\max}^2}\frac{\frac{\overline{i_n^2}}{\Delta f}}{8\Delta\omega^2}\frac{\omega_{1/f}}{\Delta\omega}\right]. \tag{4.18}$$

Equation (4.18) highlights a major contribution of this theory [93]. Phase noise resulting from flicker noise upconversion is found to be proportional to c_0, the DC component of the ISF. Hence, the $1/\Delta\omega^3$ region in the oscillator spectrum can be reduced by reducing c_0. This is contrary to the common belief that the phase noise $1/\Delta\omega^3$ corner is the same as the 1/f corner for flicker noise, since the complete spectrum close to DC is upconverted to the vicinity of the carrier. The theory, however, requires extensive simulation rather than analytical means. Also, the theory does not provide insight on minimizing phase noise by optimizing an oscillator topology [93].

4.4.5 Hegazi Rael and Abidi

This theory treats the active elements of the oscillator as a mixing pair that causes the upconversion of the noise sources of the tank and of the active devices [74]. Passive LC filters were added to the bias current sources to lower phase noise. The phase noise can be given by the Leeson-like formula:

$$\mathcal{L}(\Delta\omega) = \frac{4FKTR_P}{V_0^2}\left(\frac{\omega_c}{2Q_{\tan k}\Delta\omega}\right)^2 . \tag{4.19}$$

The factor F can be given by:

$$F = 2 + \frac{8\gamma R_p I_T}{\pi V_0} + \gamma\frac{8}{9} g_{mbias} R . \tag{4.20}$$

where R_p refers to the parallel resistance of the tank, V_0 refers to the amplitude over the tank, I_T is the tail bias current, g_{mbias} is the current source transconductance and γ is the FET noise factor (2/3 for long channel devices). Similar to Lesson's conclusions, this theory predicts the dependence of phase noise on the LC tank quality factor.

4.5 Integrated LC oscillators

4.5.1 LC oscillators

Several oscillator topologies have been presented in the literature. Structures including an NMOS-only core [94], PMOS only core or cross-coupled structures including NMOS and PMOS transistors were presented [95]–[97]. The cross-coupled differential oscillator consumes more power and occupies more die area. However, the NMOS-only oscillator was shown to exhibit inferior phase noise at all the measured bias points [95]–[97]. There are several reasons for the superiority of the complementary structure over the all-NMOS structure. The complementary structure offers higher transconductance for a given current, which results in faster switching of the cross-coupled differential pair. This structure also offers better rise- and fall-time symmetry, which results in less upconversion of flicker noise [71], [97]. A drawback of the differential LC oscillator topology is the limited headroom for signal swing, which makes this topology less suitable for low voltage operation. Each of the LC oscillator topologies can be augmented by a bias current source as shown in Figure 4-5. The tail current source can be implemented in either PMOS or NMOS devices. PMOS current source implementations are usually preferred as PMOS devices have lower flicker noise for a given bias current [8]. The tail current source controls whether the oscillator operates in the so-called *voltage limited* or *current limited* regimes [95]. On the other hand, the tail current source limits the voltage swing across the tank and adds noise to the overall VCO noise [71], [95]. Hegazi *et al.* [74] reduced the noise contribution from the tail current source using passive filters. An advantage of a tail current source is that it sets the bias for the differential pair making it more immune to supply voltage variations.

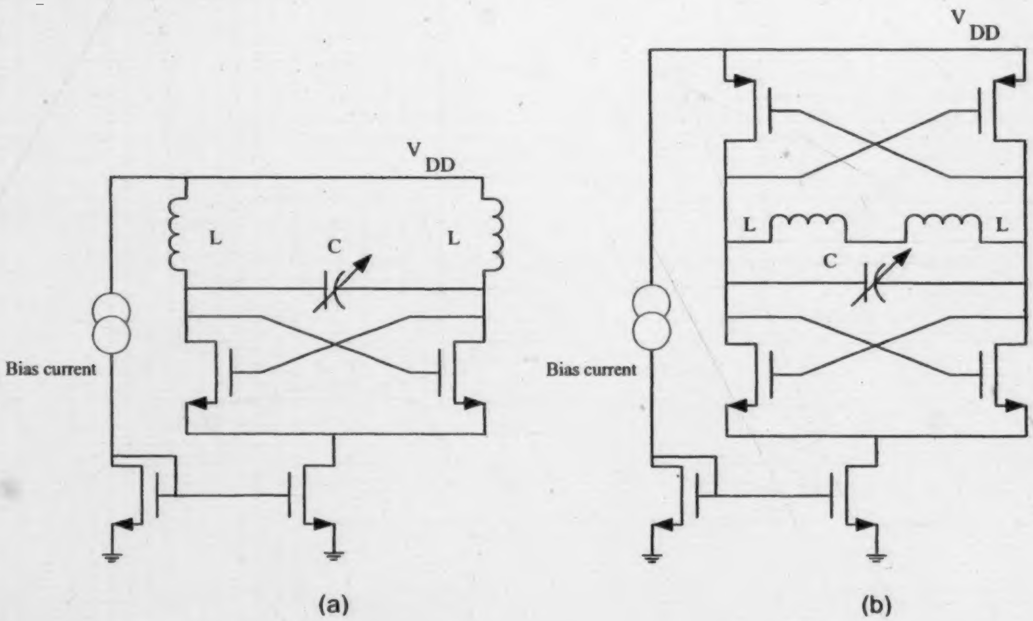
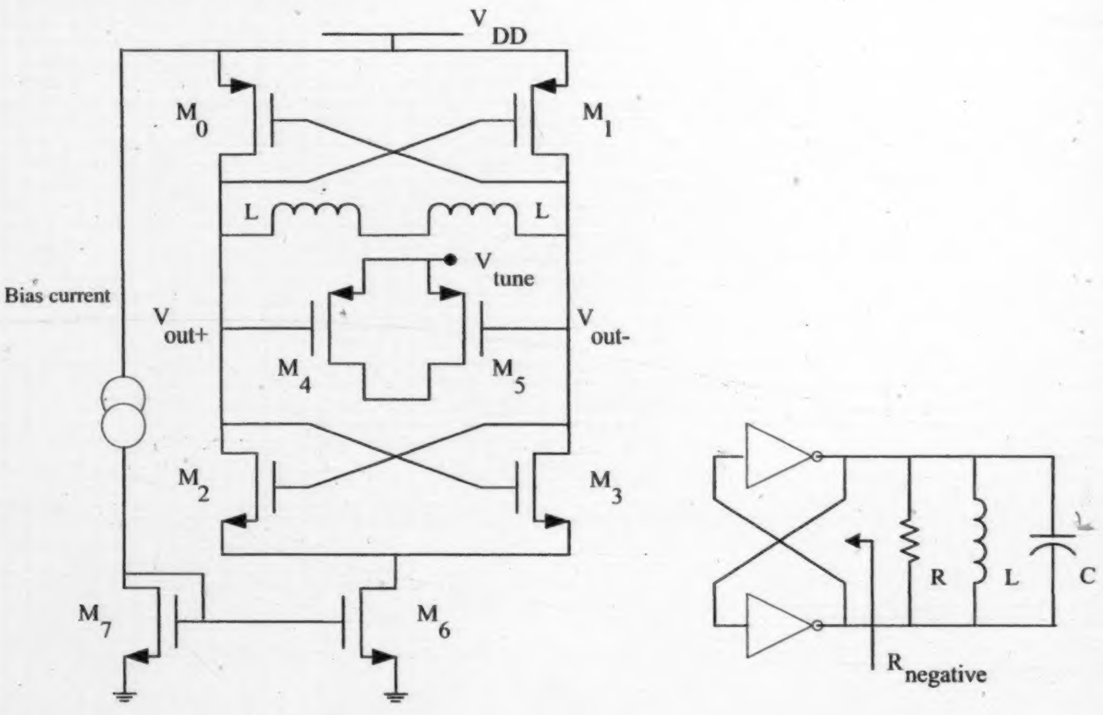


Figure 4-5: (a) NMOS-only differential oscillator; (b) NMOS and PMOS differential.

4.6 LC VCO circuit design

In this section we describe the design of LC oscillators. First, the conditions necessary for the start of oscillation are described. Then, the tradeoffs involved in the design of integrated inductor are highlighted.

4.6.1 Transconductor Design


V_{DD}
M_0
M_1
L
L
V_{tune}
Bias current
V_{out+}
V_{out-}
M_4
M_5
M_2
M_3
M_7
M_6
R
L
C
$R_{negative}$

(a) (b)

Figure 4-6: (a) Cross-coupled differential inverter oscillator; (b) Representation using inverters.

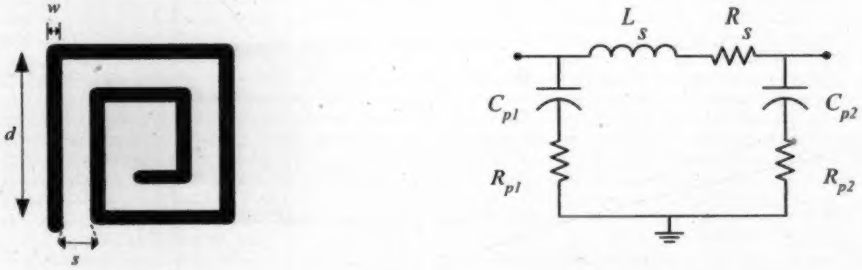
The complementary oscillator shown in Figure 4-6.a can be considered as a cross-coupled pair of inverters in parallel with a tank circuit shown in Figure 4-6.b [96], [97]. The complementary oscillator shown in Figure 4-6.a can create twice the negative resistance of its single-sided counterparts for a given bias current, because the same bias current is used in both PMOS and NMOS devices. The negative resistance seen by the tank circuit is given by [97]:

$$R_{negative} = \frac{2}{g_{m,n} + g_{m,p}}, \tag{4.21}$$

where $g_{m,n}$ and $g_{m,p}$ are the transconductances of NMOS and the PMOS devices, respectively. Since the oscillator is essentially a pair of cross-coupled inverters, the DC level of the tank voltages will be the switching point of each inverter. Thus, if $|R_{negative}|$ is greater than or equal to the equivalent parallel resistance of the tank, the circuit will oscillate. The differential pair can be modeled as a current source switching between I_{tail} and $-I_{tail}$ in parallel with a resistance–inductance–capacitance (*RLC*) tank. A simple expression for the tank voltage amplitude can be obtained assuming that the current in the differential stage switches quickly from one side to another. Harmonics of the input current are strongly attenuated by the *LC* tank, leaving the fundamental of the input current to induce a differential voltage swing amplitude of $(4/\pi)I_{tail}\,R_{eq}$ across the tank if one assumes a rectangular current waveform [97]. R_{eq} is the equivalent parallel resistance of the tank. The frequency of oscillation can be calculated from the linear model given in [79].

Low power, low phase noise LC oscillator design entails several tradeoffs. As seen from equation (4.19), increasing the amplitude of oscillation or improving the inductor quality factor can improve the LC oscillator phase noise. However, as mentioned in sections 4.5.1 and 4.6.1, for operation in the current limited regime, an increase in oscillation amplitude can be realized by spending more power. The quality factor can be improved by increasing the inductance. However, increasing the inductance entails a tradeoff between occupied die area and tuning range as described in the next section.

4.6.2 Inductor design



(a)

(b)

Figure 4-7: Square spiral inductor: (a) Layout; (b) Equivalent circuit.

Among the important parameters of integrated inductors are quality factor, self-resonance frequency, and inductor area. These parameters depend strongly on the layout of the inductor and the properties of the technology. Inductors are usually implemented as spiral structures [100]. The bulk of the spiral is implemented in the topmost available metal as this layer has the lowest metal resistance and lowest capacitance to the substrate. The connection to the center of the spiral is made with a lower metal layer. In LC oscillator design a large value of inductance is desired in order to maximize the equivalent parallel resistance of the LC tank. Increasing this resistance lowers power consumption since the transconductances required for oscillations become smaller. In addition to the loss of die area, maximizing the value of the inductor entails two trade-offs. First, due to the increased parasitic capacitances of the inductor, the self-resonance frequency decreases, approaching the oscillation frequency of interest. Second, the tank capacitance becomes limited by inductor parasitic capacitances making it difficult to vary the oscillation frequency using varactors. Thus, a compromise between inductor value and area is usually necessary. Several techniques have been proposed to improve the inductor quality factor [100]–[103]. These techniques were focused on reducing the losses caused by either the metal series resistance or the lossy conductive substrate. In [101], a method based on shunting several metal layers was proposed to reduce inductor series resistance. However, this technique suffers from increased capacitance between the inductor and the substrate due to the proximity of the metal layers to the conductive substrate. Inductors realized using bond wires achieved high Q but suffered from lack of reproducibility for manufacturing. Yue and Wong [102] have shown that losses in the substrate can be reduced when the value of the resistance R_p shown in Figure 4-7.b goes to either zero or infinity. This is an important observation because it implies that Q can be improved by making the silicon substrate either short or open. Using high resistivity silicon or etching away the substrate is equivalent to making the substrate an open circuit. This approach was used by Burghartz *et al.* [101]. Yue and Wong [102] investigated shorting the substrate using a ground shield placed between the inductor and the conductive substrate. This technique lead to around 33% improvement in Q.

The inductance of a square spiral inductor can be approximated by [8]:

$$L \approx 4\pi\mu_0 n^2 r = 1.2*10^{-6} n^2 r, \qquad (4.22)$$

where L is the coil inductance, r the coil radius in meters, μ_0 is the permeability of free space and n is the number of turns. The inductors used in the VCO shown in Figure 4-6 were optimized using the tool "Analysis and Simulation of Spiral Inductors and Transformers for ICs" (ASITIC) [100]. The layout of a square spiral inductor is shown in Figure 4-7.a. The number of turns n, metal width w, metal spacing s, and inductor outer diameter d characterize the spiral. A nonsymmetric equivalent circuit for spiral inductors used in simulations is depicted in Figure 4-7.b. The inductance and resistance of the metal traces are given by L_s and R_s, respectively. R_p and C_p give the substrate resistance and capacitance, respectively.

4.7 Conclusion

Phase noise theories cited in the literature were reviewed in this chapter. Over several decades, researchers have made contributions to phase noise theories using either discrete or integrated devices. Each proposed model sheds some light but no method covers all aspects of phase noise modeling. Phase noise theories developed by researchers using discrete devices emphasize optimum matching between the active device and the resonator. A correlation between oscillator phase noise and the amplifier low frequency noise was established by Llopis *et al.* [67]. Research using integrated devices emphasizes optimum conditions for injecting noise to the resonator. Another approach suggests adding filters to the bias current source to lower phase noise.

Chapter 5

Coupled Oscillators in CMOS Technology

5.1 Introduction

Many modern transceiver architectures require signal sources that generate quadrature or polyphase signals as mentioned in chapter one. The problem of generating RF sinusoidal signals in quadrature can be considered in this thesis as follows: There are two nonlinear self-sustained periodic oscillators, and these two oscillators interact through coupling [78]. An emphasis is placed on selecting the technique, type, and strength of coupling in order to generate accurate quadrature signals. The term "coupling technique" describes the network used as the coupling element. The coupling network can be implemented using either passive or active networks. The term "coupling type" refers to the harmonic used by the coupling network to establish the coupling process between oscillators. Either odd or even harmonics can be used to couple oscillators. The strength of coupling can be defined by the influence of the coupling term on the differential equation describing each oscillator. Several methods exist to generate quadrature signals as will be shown in section 5.2 [104]–[116]

For quadrature generation, the self-oscillating nonlinear systems presented in the literature include the Robinson type, van der Pol oscillators, and relaxation oscillators. Characteristics of Robinson type oscillators and van der Pol oscillators are compared in [117]. Relaxation oscillators are also widely used in on-chip applications as they provide considerable die area reduction compared to LC oscillators. However, stand-alone relaxation oscillators are known to have worse phase noise performance than LC oscillators. Indeed, LC oscillators have better phase noise performance, but when they are coupled to obtain quadrature outputs there is some phase noise degradation [115]. Comparison of quadrature signal generation using relaxation and Robinson type oscillators was done in [118]. The effects of coupling on phase noise in LC oscillators has been discussed in [105], [118] and [119]. Phase noise of multiphase LC oscillators was studied using a linear model in [105]. Rohde *et al.* [59] used a simple oscillator model to prove that coupling improves the phase noise of LC oscillators. However, the main outcome of the study done by [105] was that the resonator phase shift must be minimized in order to reduce the coupled oscillators' phase noise. The theory developed in [105] was confirmed by the design of a 5 GHz I/Q LC oscillator including a phase shifter to improve the coupled oscillator phase noise.

This chapter is organized as follows: In section one, different methods of generating quadrature signals are reviewed. In section two, a general synchronization system using coupling types and techniques for LC oscillators discussed above is presented. The development of quadrature mutually coupled LC-oscillators is characterized by efforts, for first and higher harmonic coupling, to stay in the frame of linear theory [105], [112]. Yet, synchronization may be explained by referring to the nonlinear theory of mutual synchronization. The fact that the synchronization of LC-oscillators is a deeply nonlinear phenomenon was known long ago [121]. But these results are overlooked in the modern approach to the problem of synchronization. The correct, full explanation of synchronization, based on the nonlinear behavior of constituent oscillators, is absent. In section three, equations for the calculation of amplitude and frequency of coupled van der Pol oscillators are derived [120], [121]. In previous sections, we considered coupling in purely deterministic oscillators, neglecting the effects of noise. In section four, the effects of coupling on coupled LC oscillators' phase noise will be discussed. Coupled RC oscillators are discussed in section five. In section six, the effects of coupling strength on phase noise and quadrature errors in coupled relaxation oscillators and LC oscillators are studied experimentally using a 5 GHz oscillator built in 0.18 μm TSMC technology.

5.2 Methods of quadrature signal generation

Several techniques to generate quadrature signals have been presented in the literature as shown in Figure 5-1 [59], [112]. Ring oscillators were used to generate polyphase signals in [106]. This type of implementation occupies a small die area and has a large tuning range due to the absence of resonant tuned circuits. However, this implementation has the disadvantage of poor phase noise performance and large power consumption. An LC voltage controlled oscillator (VCO) followed by a RC-CR filter or a polyphase filter can be used for quadrature signal generation as shown in Figure 5-1.b. The driving LC oscillator provides adequate phase noise signals but the oscillator tuning range is low due to the LC circuit limited bandwidth. Another serious disadvantage of using this implementation in transceivers is the fact that the oscillators run at almost the same frequency as the power amplifier which causes the oscillator to be susceptible to pulling. An oscillator running at half local oscillator frequency can be implemented to avoid the oscillator-pulling problem. A frequency doubler follows the main oscillator as shown in Figure 5-1.c. A drawback of this implementation is the power consumed by the frequency doubler [104]. The solution shown in Figure 5-1.d suggests running the VCO at double or quadruple the frequency required for the quadrature signals [107], [108]. In this implementation, a frequency divider generates the required quadrature signals. The frequency divider can be implemented using a divide by 2-master/slave toggle flip-flop. A drawback of this implementation is the power consumed by the extra circuitry needed for frequency division. In most of the polyphase oscillators presented in the previous section, active elements were used as coupling circuits [112]–[115]. In addition, using passive circuits to couple two oscillators was suggested in [105] and [116]. Each of these coupling types suffers from some disadvantages. For example, while implementing coupling using active circuits increases power consumption, using passive devices as coupling elements increases the occupied die area.

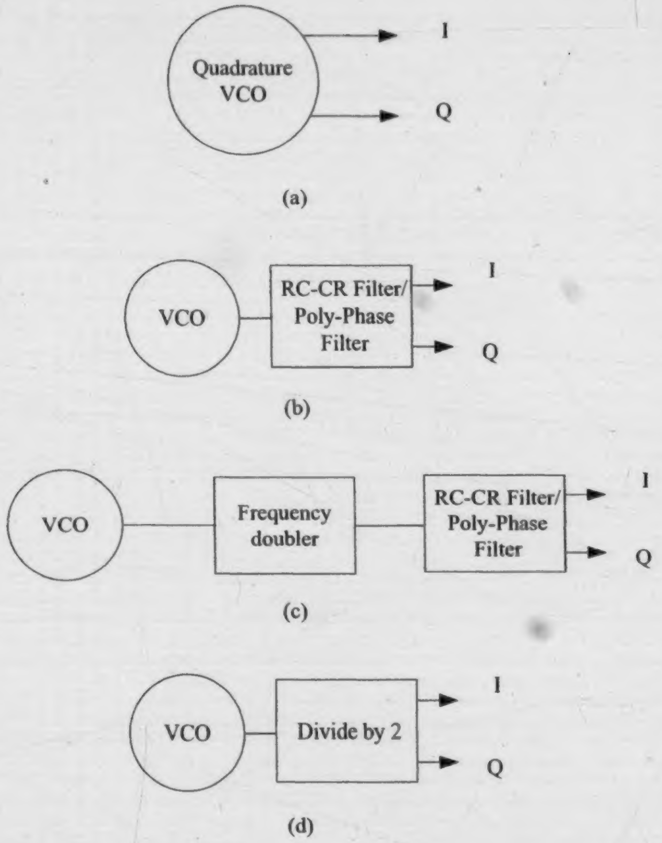
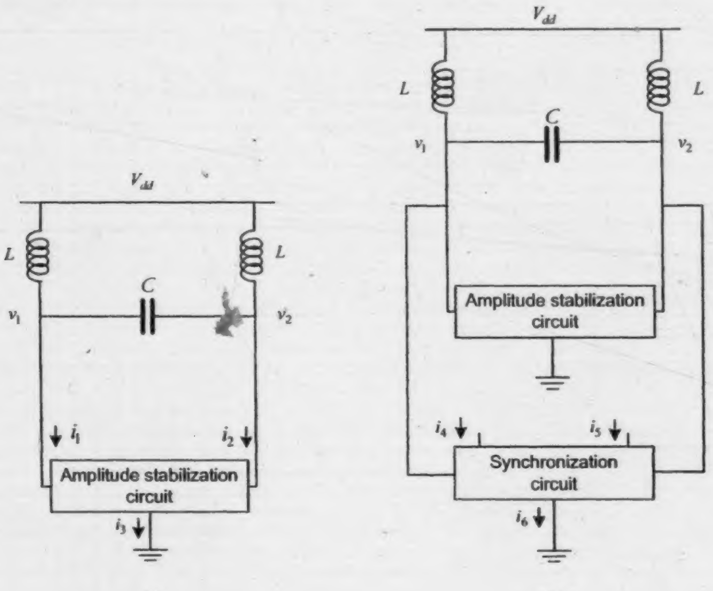

Quadrature VCO
I
Q
(a)
VCO
RC-CR Filter/ Poly-Phase Filter
I
Q
(b)
VCO
Frequency doubler
RC-CR Filter/ Poly-Phase Filter
I
Q
(c)
VCO
Divide by 2
I
Q
(d)

Figure 5-1: Different methods of generating quadrature signals [104].

5.3 Block diagram study of coupled LC oscillators

Consider that two oscillators of the type shown in Figure 5-2.a are being synchronized. Each oscillator consists of an LC circuit and an amplitude stabilizing circuit. We will assume symmetric oscillators and symmetric amplitude stabilization circuits. A coupling circuit augments the main oscillator as shown in Figure 5-2.b. It is possible to show that the process of amplitude stabilization is connected with the creation of harmonic distortions in the currents i_1 and i_2. The differential current $i_d = i_1 - i_2$ supplied to the LC circuit, in addition to the first harmonic, includes the third and other odd harmonics. The current $i_3 = i_1 + i_2$ includes a DC component and a second and other even harmonics. Coupling or synchronization circuits can be added to the two oscillators. The coupling circuit may operate on odd (including the first harmonic) or even harmonics. In the case of using odd harmonics, the harmonics produced in the first oscillator control the operation of the second oscillator. This phenomenon is especially clear in the case of active coupling using the first harmonic. Use of even harmonic coupling is similar. The current i_3 can be used for second harmonic coupling. Second harmonic coupling circuits may also operate on the current i_6 as shown in Figure 5-3. Odd harmonic synchronization can be implemented using the synchronization circuit operating on the currents i_4 and i_5. Most of the coupling circuits used in [106]–[111] were implemented using the first or odd harmonics. The second harmonic common mode coupling type was presented in [122], [123]. The coupling was realized using passive narrowband networks. The main advantage of this second harmonic coupling is that, as the coupling circuit is not connected to the LC circuit nodes, it will not force any additional change in the synchronized oscillation frequency. Therefore, there will be no additional phase noise degradation due to further shifts from the resonant frequency [124]. One drawback of such realization is the extra die area required to implement the passive devices. To avoid the drawback of the area increase found in [122], Filanovsky *et al.* [125] presented a new coupling technique to realize the second harmonic coupling type to enforce a quadrature relation between the two van der Pol (VDP) oscillators. This new technique suggested using active elements as the main coupling block in a second harmonics quadrature oscillator. In [125], the circuit implementation and the conditions of establishing a strong second harmonic component in the common mode current were derived, and the benefits and drawbacks of the new coupling technique were highlighted. Another combination of coupling types was suggested in [126]. Using weak first harmonic coupling (as no bias current is consumed by the coupling circuits) and second harmonic coupling (using a passive narrow band circuit) yields a benefit from the good phase noise performance of a single LC oscillator and, at the same time, achieves accurate quadrature outputs.


V_{dd}
L
L
C
v_1
v_2
i_1
i_2
Amplitude stabilization circuit
i_3
V_{dd}
L
L
C
v_1
v_2
Amplitude stabilization circuit
i_4
i_5
Synchronization circuit
i_6

(a) (b)

Figure 5-2: LC oscillator (a) without and (b) with synchronization circuit.

It can be concluded from the above description of coupling mechanisms that coupling and synchronization are closely connected with phase locking and entrainment. Yet, although the nonlinear nature of the last phenomenon is well recognized, the nonlinear nature of synchronization is not recognized. Attempts to solve synchronization phenomena using linear methods do not provide an adequate description of this phenomenon.

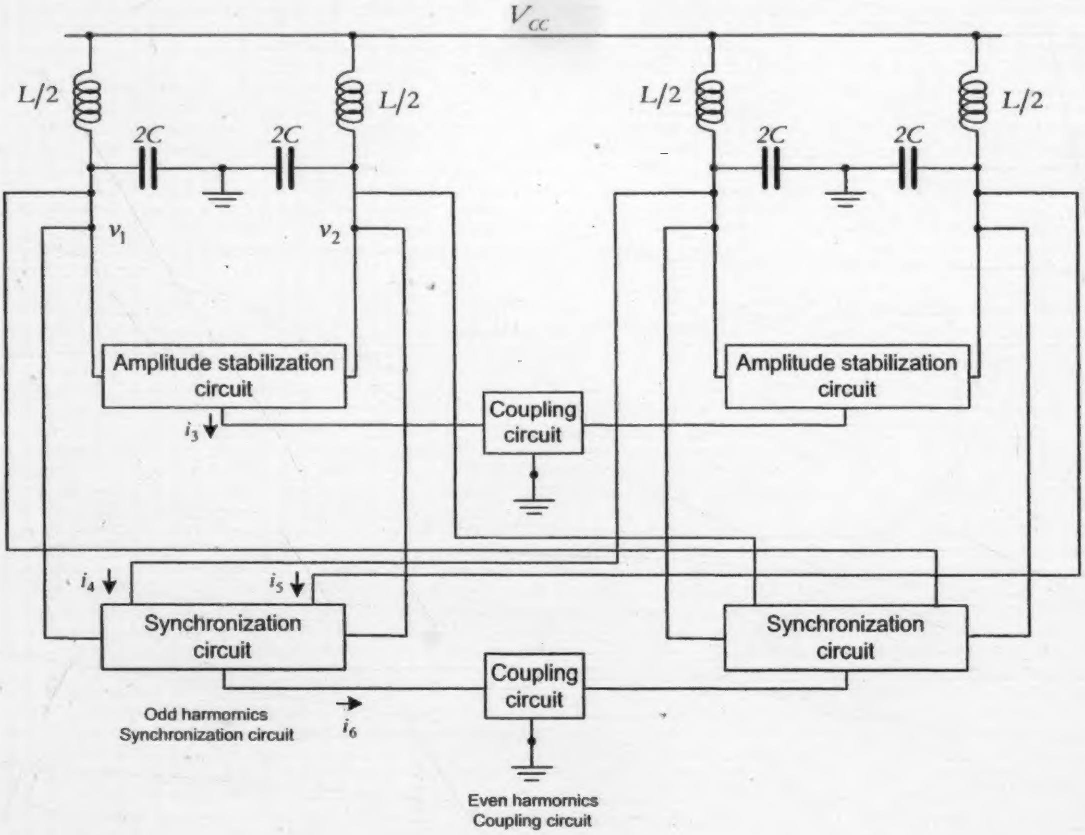

V_{CC}
L/2
L/2
L/2
L/2
2C
2C
2C
2C
v_1
v_2
Amplitude stabilization circuit
Amplitude stabilization circuit
Coupling circuit
i_3
i_4
i_5
Synchronization circuit
Synchronization circuit
Coupling circuit
i_6
Odd harmomics Synchronization circuit
Even harmomics Coupling circuit

Figure 5-3: Synchronization using odd and even harmonics.

5.4 Coupled LC oscillators

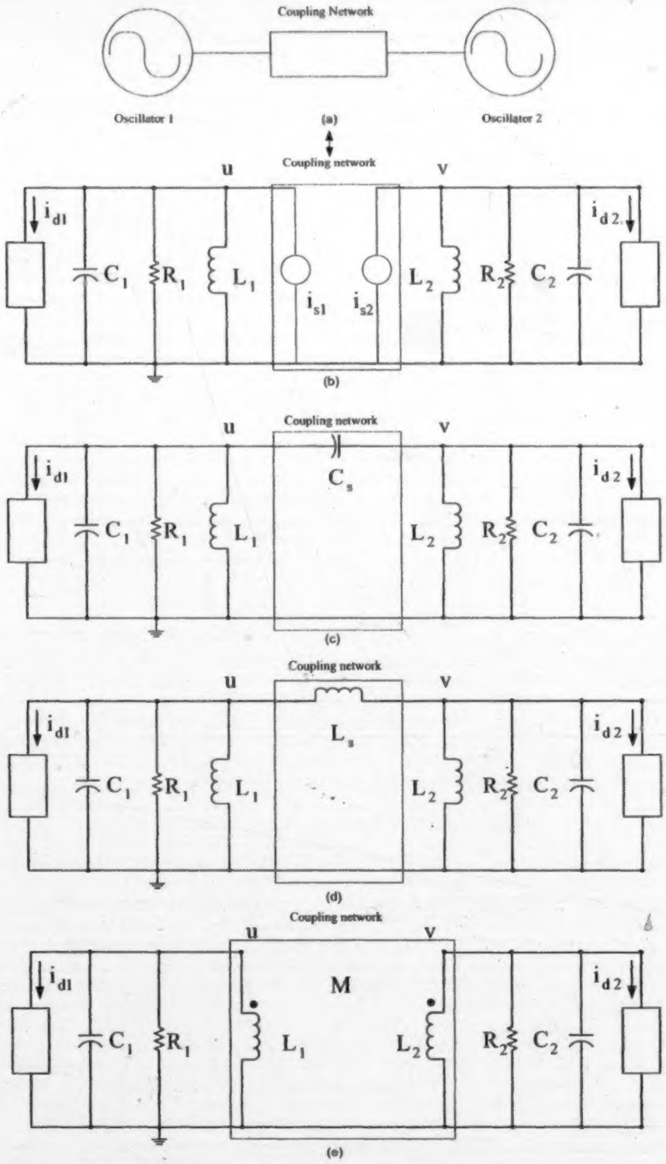

Coupling Network
Oscillator 1
(a)
Oscillator 2
u
Coupling network
v
i_d1
C_1
R_1
L_1
i_s1
i_s2
L_2
R_2
C_2
i_d2
(b)
u
Coupling network
v
C_s
i_d1
C_1
R_1
L_1
L_2
R_2
C_2
i_d2
(c)
Coupling network
u
v
L_s
i_d1
C_1
R_1
L_1
L_2
R_2
C_2
i_d2
(d)
Coupling network
u
v
M
i_d1
C_1
R_1
L_1
L_2
R_2
C_2
i_d2
(e)

Figure 5-4: Quadrature oscillator with (a) coupling transconductances; (b) capacitive coupling; (c) Inductive coupling and (d) transformer coupling.

A block diagram of two stand-alone oscillators and the coupling network is shown in Figure 5-4. Mutual coupling is achieved using transconductances connecting the oscillators as shown in Figure 5-4.a [112]–[116]. Stand-alone oscillators can also be coupled using passive devices such as capacitors, inductors, and transformers as shown in Figures 5-4.c, 5-4.d, and 5-4.e, respectively [116]. However, compared to inductive and capacitive coupling, coupling using transconductances offers several benefits. For instance, coupling using transconductances is more area efficient than coupling using passive devices. Also, coupling using transconductances is more suitable for RC oscillators, as passive devices might interfere with the frequency setting elements of RC oscillators. When two or more van der Pol oscillators are interconnected with mutual coupling, an entrainment condition is obtained similar to the well-known phenomenon of forced entrainment [120], [121]. As shown in [121], the type of coupling affects the frequency and amplitude of the coupled oscillators. In this section, the equations for calculation of the synchronization frequency, and the equations for the oscillation amplitudes in both oscillators are derived. It is shown that, in the general case, the synchronization frequency is different from the frequencies of noncoupled oscillators. The oscillation amplitudes are also not equal: one oscillator (with larger power) becomes a master, and has frequency and oscillation amplitude close to the values that existed before coupling. The other oscillator becomes a slave, and its frequency and amplitude are defined by the oscillation parameters of the master oscillator and the coupling coefficients. The structure of this section is the following. Subsection 5.4.1 gives the synchronization theory. The amplitude and frequency of the coupled oscillators are derived in subsection 5.4.2. A study of the effects of coupling on phase noise and quadrature errors is presented in section 5.4.3.

5.4.1 Synchronization theory of LC oscillators

In Figure 5-4.b, two oscillators are modeled with the tank circuits L_1, R_1, C_1, and L_2, R_2, C_2, respectively; also, each oscillator model includes a controllable current source providing compensation for losses and amplitude control. Assume that these oscillators are of the van der Pol type, with $i_{d1} = -M_1 u(1 - N_1 u^2)$ and $i_{d2} = -M_2 v(1 - N_2 v^2)$ where M_1, M_2, N_1, N_2 are positive constants [80]. The oscillators are mutually coupled through transconductances providing coupling currents $i_{s1} = g_1 u$ and $i_{s2} = g_2 v$. Then

$$\begin{cases} \dfrac{1}{L_1}\displaystyle\int u\,dt + \dfrac{u}{R_1} + C_1\dfrac{du}{dt} + i_{s1} + i_{d1} = 0 \\ \dfrac{1}{L_2}\displaystyle\int v\,dt + \dfrac{v}{R_2} + C_2\dfrac{dv}{dt} + i_{s2} + i_{d2} = 0 \end{cases} \tag{5.1}$$

After differentiation, this system of equations (5.1) can be rewritten as:

$$\begin{cases} \dfrac{d^2u}{dt^2} - 2(\delta_0 - \delta_2 u^2)\dfrac{du}{dt} + \sigma_1^{\,2} u + \alpha_1\dfrac{dv}{dt} = 0 \\ \dfrac{d^2v}{dt^2} - 2(\gamma_0 - \gamma_2 v^2)\dfrac{dv}{dt} + \sigma_2^{\,2} v + \alpha_2\dfrac{du}{dt} = 0 \end{cases} \tag{5.2}$$

where $\delta_0 = \frac{1}{2}\left(M_1 - \frac{1}{R_1}\right)\frac{1}{C_1}$ $\gamma_0 = \frac{1}{2}\left(M_2 - \frac{1}{R_2}\right)\frac{1}{C_s}$, $\delta_2 = \frac{3M_1N_1}{2C_1}$, $\gamma_2 = \frac{3M_2N_2}{2C_2}$, $\sigma_1^{\,2} = \frac{1}{L_1C_1}$, $\sigma_2^{\,2} = \frac{1}{L_2C_2}$.

The coupling coefficients are given by $\alpha_1 = -\frac{g_1}{C_1}$ and $\alpha_2 = -\frac{g_2}{C_2}$. Assume that the system (5.2) has the steady-state synchronous solution described as:

$$\begin{cases} u = A\cos\omega t \\ v = B\sin(\omega t - \varphi) = B\cos\varphi\sin\omega t - B\sin\varphi\cos\omega t \end{cases}, \tag{5.3}$$

where φ is the phase error of the quadrature outputs u and v. To find amplitudes A and B, and the frequency ω of these oscillations, system (5.2) is rewritten as:

$$\begin{cases} \dfrac{d^2u}{dt^2} + \omega^2 u = (\omega^2 - \sigma_1{}^2)u + 2(\delta_0 - \delta_2 u^2)\dfrac{du}{dt} - \alpha_1\dfrac{dv}{dt} \\ \dfrac{d^2v}{dt^2} + \omega^2 v = (\omega^2 - \sigma_2{}^2)v + 2(\gamma_0 - \gamma_2 v^2)\dfrac{dv}{dt} - \alpha_2\dfrac{du}{dt} \end{cases}. \tag{5.4}$$

Substituting (5.3) in the right side of equations (5.4) gives:

$$\begin{cases} \dfrac{d^2u}{dt^2} + \omega^2 u = \left[(\omega^2 - \sigma_1{}^2)A - \alpha_1\omega B\cos\varphi\right]\cos\omega t \\ +\left[-2A\omega(\delta_0 - \dfrac{1}{4}\delta_2 A^2) - \alpha_1\omega B\cos\varphi\right]\sin\omega t + \ldots \end{cases} \tag{5.5}$$

and

$$\begin{cases} \dfrac{d^2v}{dt^2} + \omega^2 v = \begin{bmatrix} -(\omega^2 - \sigma_2{}^2)B\sin\varphi + \\ 2\omega B(\gamma_0 - \dfrac{1}{4}\gamma_2 B^2)\cos\varphi \end{bmatrix}\cos\omega t \\ +\left[(\omega^2 - \sigma_2{}^2)B\cos\varphi + 2\omega B(\gamma_0 - \dfrac{1}{4}\gamma_2 B^2)\sin\varphi\right]\sin\omega t + \ldots \end{cases}. \tag{5.6}$$

In steady-state oscillations, substitution of (5.3) makes the left side of equations (5.5) and (5.6) equal to zero. This solution is also possible if the coefficients before $\sin\omega t$ and $\cos\omega t$ terms in equations (5.5) and (5.6) are equal to zero. This gives the following system of equations:

$$\begin{cases} (\omega^2 - \sigma_1{}^2)A - \alpha_1\omega B\sin\varphi = 0 \\ -2\omega A(\delta_0 - \dfrac{1}{4}\delta_2 A^2) + \alpha_1\omega^2 B\sin\varphi = 0 \\ -(\omega^2 - \sigma_2{}^2)B\sin\varphi + 2\omega B\cos\varphi(\gamma_0 - \dfrac{1}{4}\gamma_2 B^2) = 0 \\ (\omega^2 - \sigma_2{}^2)B\cos\varphi + 2\omega B\sin\varphi(\gamma_0 - \dfrac{1}{4}\gamma_2 B^2) + \alpha_2 A\omega = 0 \end{cases} \tag{5.7}$$

This solution can be rearranged in terms of amplitude and quadrature error as:

$$\begin{cases} A = 2\sqrt{\dfrac{\delta_0 + \dfrac{\alpha_1}{2}\dfrac{B}{A}\sin\varphi}{\delta_2}} \\ \omega^2 - \sigma_1^2 = \alpha_1 \omega \dfrac{B}{A}\cos\varphi \\ \omega^2 - \sigma_2^2 = -\alpha_2 \omega \dfrac{A}{B}\cos\varphi \\ B = 2\sqrt{\dfrac{\gamma_0 + \dfrac{\alpha_2}{2}\dfrac{A}{B}\sin\varphi}{\gamma_2}} \end{cases} \tag{5.8}$$

Different cases of coupling such as coupling using capacitors, inductors, and transformers can be included by modifying equations (5.2) using [116]:

$$\begin{cases} \dfrac{d^2u}{dt^2} - 2(\delta_0 - \delta_2 u^2)\dfrac{du}{dt} + \sigma_1{}^2 u + \alpha_1 f_1(v) = 0 \\ \dfrac{d^2v}{dt^2} - 2(\gamma_0 - \gamma_2 v^2)\dfrac{dv}{dt} + \sigma_2{}^2 v + \alpha_2 f_2(u) = 0 \end{cases} \tag{5.9}$$

5.4.2 Synchronization characteristics

Multiplying the second and third equations of (5.8), the frequency of synchronized oscillations can be calculated from the following equation:

$$\left(\omega^2 - \sigma_1^2\right)\left(\omega^2 - \sigma_2^2\right) - \alpha_1\alpha_2\omega^4 \sin^2\varphi = 0\,. \tag{5.10}$$

Equation (5.10) shows that the synchronized frequency is less than σ_1 or larger than σ_2. If the oscillation amplitudes of noncoupled oscillators are A_0 and B_0, and if $A_0 >> B_0$, in other words, oscillator *A* develops more power than oscillator *B*, then the first two equations of (5.8) give:

$$\begin{cases} A \approx 2\sqrt{\dfrac{\delta_0}{\delta_2}} = A_0 = const \\ \omega \approx \sigma_1 \end{cases} \tag{5.11}$$

Hence, the amplitude and frequency of the oscillator with more power are preserved. This oscillator becomes a master and enslaves another oscillator. The oscillator with more power, thus, can be considered as the synchronizing source entraining the oscillator with less power. Rohde *et al.* [105] assume that the second oscillator starts to oscillate due to the injection mechanism from the first oscillator. The amplitude and frequency of the oscillator with less power are calculated using the third and forth equations of (5.8).

5.4.3 Coupled LC oscillators—Implementation

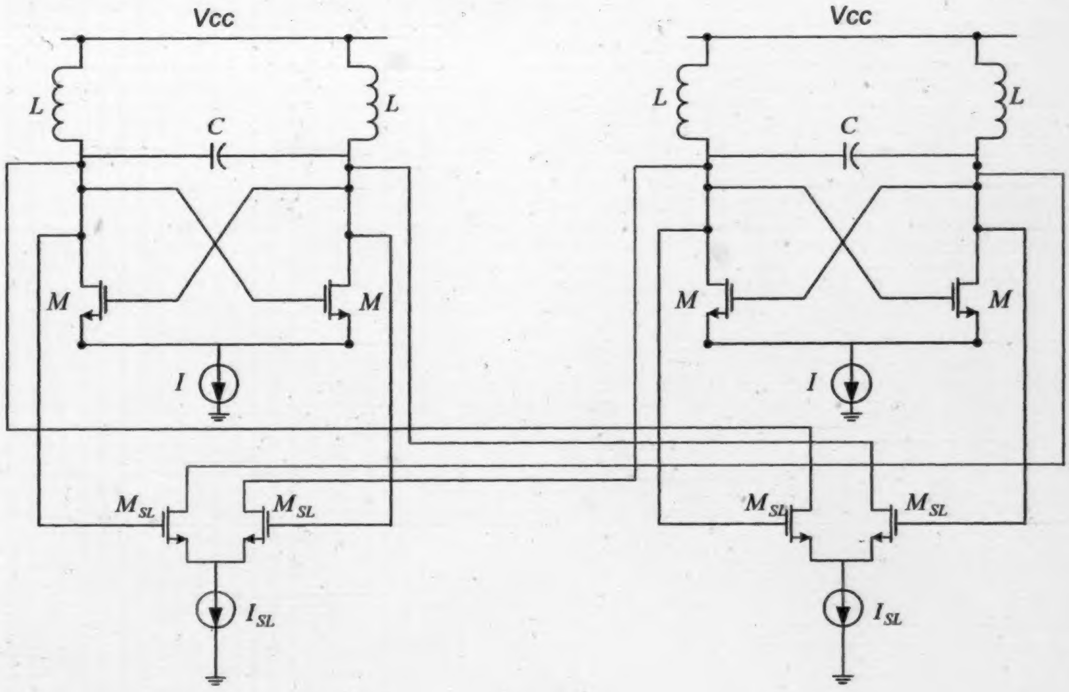


Figure 5-5: Quadarure LC oscillator schematic.

The schematic shown in Figure 5-5 can be used to implement an LC quadrature oscillator. The core of each oscillator is the NMOS cross-coupled transistor pair. The oscillator core can be considered as a negative resistance that compensates for losses of the LC circuit. A differential pair couples the two oscillators by sensing one oscillator voltage output and injecting a corresponding current into the second oscillator. A soft limiter block can represent the differential pair as will be shown in section 5.5.1. The simple linear model shown in Figure 5-6 can be used to model phase noise and quadrature accuracy in a multistage oscillator [127]. In Figure 5-6, the oscillator core is represented by the transconductance G_m, which compensates for losses introduced by the resistor R_p. The coupling transconductance is represented by G_{mc}. The current I_n and the voltage V_n represent the current and the voltage over the nth tank, respectively. The coupling strength m is the ratio of the coupling transconductance to the core transistor transconductance [127]:

$$m=\frac{G_{mc}}{G_m}. \tag{5.12}$$

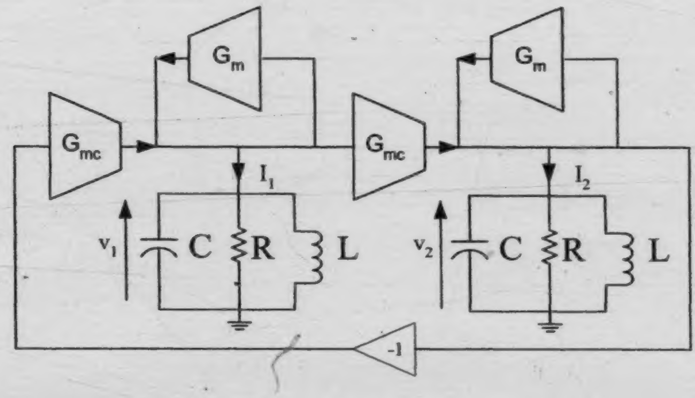


Figure 5-6: Block diagram of a quadrature oscillator.

The phase noise at an offset frequency ω_m can be given by [127]:

$$\mathcal{L}(\omega_m) = \frac{KT}{C}\frac{\omega_{osc}}{Q}\frac{1+m^2}{2}\frac{1}{\omega_m^2}\frac{1+F_Q}{A_0^2}, \tag{5.13}$$

where K is the Boltzmann constant, T is the absolute temperature, Q is the LC tank quality factor, f_{osc} is the oscillator frequency. The factor F_Q is given by $(1+m)F$, where F is the noise factor of the stand-alone oscillator. Equation (5.13) indicates that coupling worsens the phase noise performance of quadrature LC oscillators.

The use of center-tapped inductors to design LC oscillators is reported in the literature [74]. The center-tapped inductor provides an area reduction compared to the same inductance realized using the square spiral inductor shown in Figure 4-7. Due to area reduction, substrate losses are reduced, leading to an improved quality factor. As seen from equation (5.13), a higher quality factor causes an improvement in phase noise. However, designing center-tapped inductors requires powerful electromagnetic simulators. The inductors used in the coupled oscillators shown in Figure 5-5, were designed using square spiral structures due to the limitations of ASITIC.

Varactors are used as tuning elements in LC oscillators [74]. Flicker noise upconversion and thermal noise produced by varactors increase LC oscillator phase noise [74]. Effects of coupling strength on varactor contributions to LC oscillator phase noise were not measured in the current study.

5.4.4 Effects of coupling strength on phase noise in LC oscillators

For the purpose of comparison of the effect of coupling in relaxation oscillators and LC oscillators, a 5 GHz LC cross-coupled oscillator was designed. The cross-coupled oscillator shown in Figure 5-5 was designed, in a 0.18 μm CMOS technology with an oscillation frequency of 5 GHz. The circuit parameters are: for M transistors, (W/L) = 100 μm/0.18 μm, and for M_{SL}, (W/L) = 100 μm/0.18 μm. The inductor has a quality factor of 10. The coupled LC oscillator draws 1 mA from a 1.8 V supply. The simulation was done using Spectre RF considering ideal current sources. Using ideal current sources allows one to study the effects of other coupled oscillators parameters such as the coupling strength on the coupled oscillators' performance. Figure 5-7 shows that the effect of coupling strength on LC oscillator performance. In a stand-alone oscillator the phase noise is –131.6 dBc/Hz @10 MHz. With weak coupling there is an improvement of 3 dB. But with strong coupling (improving the quadrature relationship) the phase noise increases to –123.9 dBc/Hz@10 MHz. The strong cross coupling shifts the frequency of each single LC oscillator, and after locking, the two oscillators operate at a frequency that is different from their free running frequency (ω_0). This result indicates that the oscillators are operating at a frequency where the effective quality factor (Q) of each oscillator is lower than the value of Q at ω_0. The slight increase in phase noise with weak coupling might be due to the fact that the oscillators were initially operating at a frequency where the quality factor is a maximum. However, an improvement in phase noise with increased coupling was not observed in the LC oscillator as will be shown in section 5.5.3.2.

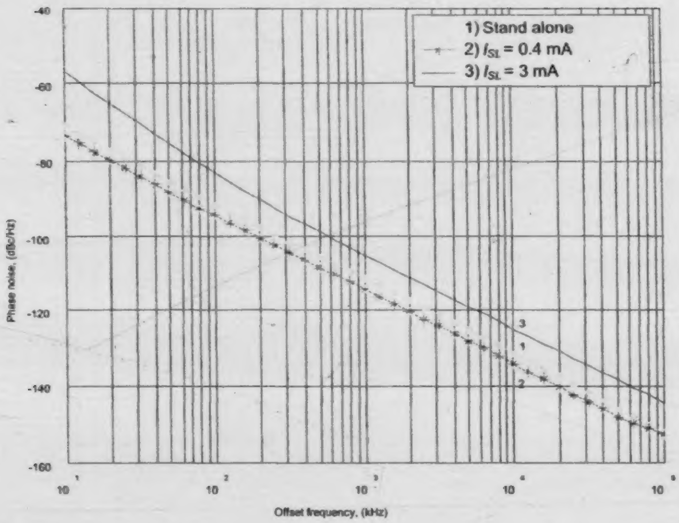
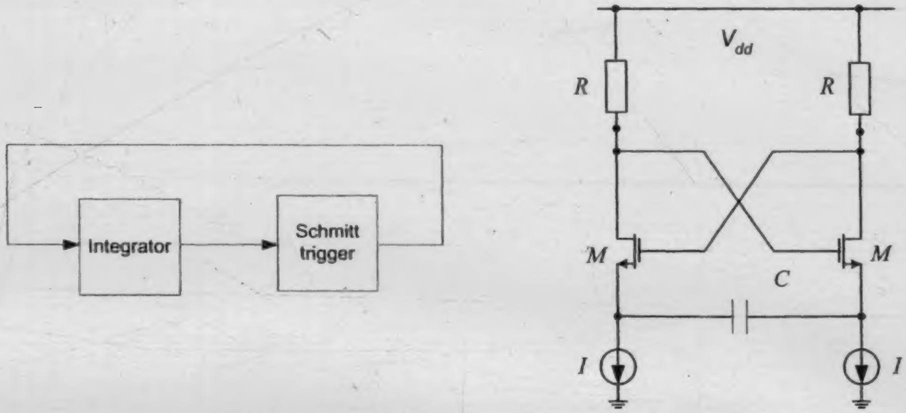


Figure 5-7: Influence of coupling on phase noise of an LC oscillator.

5.5 Coupled RC oscillators

5.5.1 Coupled RC oscillators—Implementation

Relaxation oscillators have been widely used to generate quadrature signals [128]–[133]. Relaxation oscillators generate time varying periodical output by alternating charging and discharging a timing capacitor between two threshold levels. An integrator and a Schmitt trigger can be used to model a relaxation oscillator as shown in Figure 5-8.a [130]. The Schmitt trigger generates reference levels, compares the integrator output with the reference level, and switches the sign of the integration constant. A transistor level implementation of the relaxation oscillator is shown in Figure 5-8.b. The integrator in the block diagram is realized by a capacitor and the cross-coupled transistors represent the Schmitt trigger. The bias current for the Schmitt trigger is used as the integration constant, and the voltage drop caused by the bias currents across the resistors is used as the reference signal. The Schmitt trigger compares the capacitor voltages with threshold levels and reverses the direction of the capacitor current each time a capacitor voltage crosses a threshold level [131].



(a) (b)

Figure 5-8: (a) Relaxation oscillator block diagram; (b) A practical implementation.

Figure 5-9 shows a block diagram of coupled RC oscillators. A soft limiter (an amplifier with saturation) is used to couple the two RC oscillators. The integrator output drives the input of the soft limiter. The soft limiter output can be used to synchronize a second relaxation oscillator. This technique of cross-coupling two relaxation oscillators can be used for quadrature generation [127].

A schematic of a cross-coupled relaxation oscillator is shown in Figure 5-10. The soft limiters can be implemented by a differential pair. The differential pair input senses the capacitor voltage and the outputs of the differential pair are connected to the second relaxation oscillator.

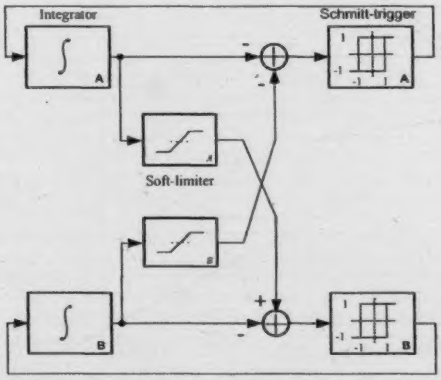

Integrator
Schmitt-trigger
A
B
Soft-limiter
1
-1
+
-

Figure 5-9: Block diagram of cross-coupled relaxation oscillator.

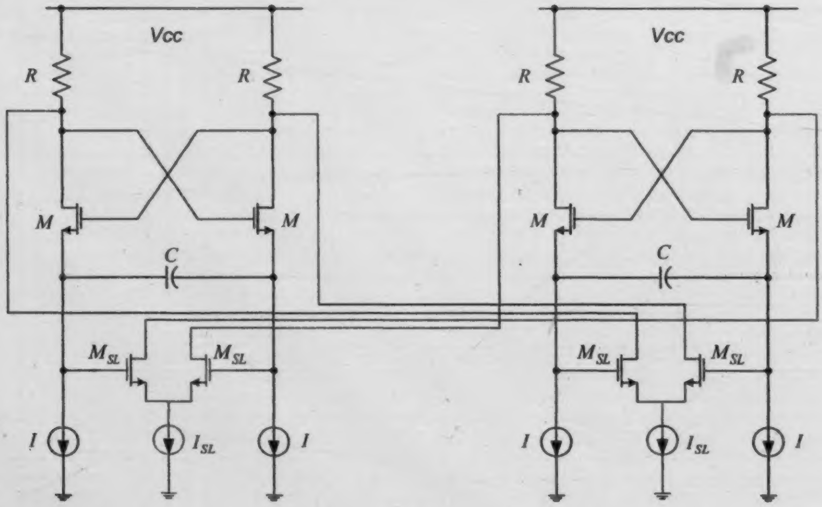

Vcc
R
M
C
M_{SL}
I
I_{SL}

Figure 5-10: Quadrature RC oscillator schematic.

The quadrature error in cross-coupled RC oscillators can be given by [128]:

$$\phi = 90^0\left(1 - \frac{\Delta I_A \Delta I_B}{I^2}\right), \tag{5.14}$$

where I is the average value of the bias current of the core oscillators' currents. ΔI_A and ΔI_B are the mismatches of the current sources in each oscillator. A drawback of RC oscillators compared to LC oscillators is a susceptibility to power supply variations. This is because the oscillation period of an RC oscillator depends on the power supply charging current.

5.5.2 Effect of coupling strength on phase noise in RC oscillator

In this section we present a simple linear model to investigate the effect of coupling on relaxation oscillators' phase noise. Figure 5-11 describes the oscillator block transfer function diagram. The Schmitt trigger in this system is a voltage-to-time converter [128]. v_{tA} and v_{tb} represent the input to the Schmitt trigger. Schmitt trigger outputs are given by ΔT_A and ΔT_B. v_{nA} and v_{nb} are two-noise sources in the Schmitt trigger inputs. Block parameters are summarized in Table 5-1.

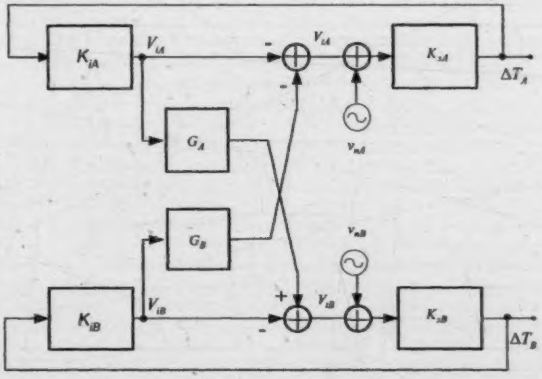


Figure 5-11: Block diagram representation of cross-coupled relaxation oscillator including noise sources.

Table 5-1: Block diagram parameters.

$K_{S\{A,B\}}$	Voltage-to-time converter factor (A or B)
$K_{i\{A,B\}}$	Time-to-voltage converter factor (A or B)
$V_{i\{A,B\}}$	Integrator output (A or B)
$\Delta T_{\{A,B\}}$	Oscillator (Schmitt trigger) output
$V_{t\{A,B\}}$	Schmitt trigger input (A or B)
$G_{l\{A,B\}}$	Soft-limiter gain (A or B)
$v_{n\{A,B\}}$	Input noise voltages (A or B)

From Figure 5-11, the following equations are obtained:

$$\begin{aligned} V_{iA} &= \Delta T_A k_{iA}, \\ V_{iB} &= \Delta T_B k_{iB}. \end{aligned} \tag{5.15}$$

The noiseless Schmitt trigger inputs are:

$$\begin{aligned} V_{tA} &= - \quad V_{iA} - V_{iB} G_B, \\ V_{tB} &= - \quad V_{iB} + V_{iA} G_A, \end{aligned} \tag{5.16}$$

where G_A and G_B may be different.

At Schmitt trigger outputs:

$$\begin{aligned} \Delta T_A &= K_{sA}\left(V_{tA} + v_{nA}\right) \\ \Delta T_B &= K_B\left(V_{tB} + v_{nB}\right) \end{aligned} \tag{5.17}$$

Solving equations (5.15) – (5.17) for ΔT_A and ΔT_B:

$$\Delta T_A \approx \frac{1}{K_{iA}K_{iB}\left(1+G_AG_B\right)}\left[K_{iB}v_{nA}+K_{iA}G_Bv_{nB}\right], \tag{5.18}$$

$$\Delta T_B \approx \frac{1}{K_{iA}K_{iB}\left(1+G_AG_B\right)}\left[K_{iA}v_{nB}+K_{iB}G_Av_{nA}\right]. \tag{5.19}$$

Equations (5.18) and (5.19) show that v_{nA} and v_{nb} are attenuated due to the feedback. Hence, to reduce the influence of internal noise in the oscillator, the coupling gain should be increased.

The cross-coupled oscillator shown in Figure 5-10 was designed, in a 0.18 μm CMOS technology with an oscillation frequency of 5 GHz. The circuit parameters are: R = 100 Ω, for M transistors (W/L) = 100 μm/0.18 μm, and for M_{SL} (soft-limiter coupling transistors), (W/L) = 100 μm/0.18 μm, C = 100 fF, I = 3 mA, and I_{SL} = 3 mA (soft-limiter coupling current). The circuit supply voltage is 3 V. The simulation was done using Spectre RF considering ideal current sources. Figure 5-12 shows the simulated phase noise for a stand-alone RC oscillator, and for the RC oscillator with coupling. It can be seen that a phase noise of –113.85 dBc/Hz @10 MHz offset is improved by 3 dB by coupling. Changing the coupling current from 0.1 mA to 3 mA further improves the phase noise performance. With I_{SL} = 0.1 mA, the simulated phase noise is –116.80 dBc/Hz @10 MHz. Increasing the coupling current to I_{SL} = 3 mA, the phase noise becomes –123.05 dBc/Hz @10 MHz. The simulation results are in accordance with theory developed by equations (5.15)–(5.19). Numerical comparison between the predictions of the theory developed and the simulation results will be considered for future work. With an increase in cross-coupling strength, coupled RC oscillators become less sensitive to noise. In this example, strong-coupled relaxation oscillators show an improvement of almost 10 dB in phase noise compared to the stand-alone oscillator.

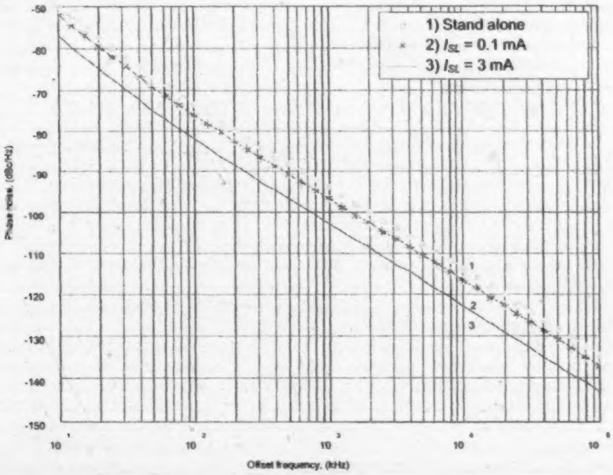


Figure 5-12: Influence of coupling on phase noise of an RC oscillator.

Comparison of coupling effects on phase noise in LC and RC quadrature oscillators is shown in Table 5-2. As seen from Table 5-2, coupling strength affects the phase noise of LC and RC oscillators differently. In LC oscillators, increasing coupling strength worsens oscillator phase noise. However, in RC oscillators, coupling improves phase noise.

Table 5-2: Phase noise (@10 MHz offset) of the LC and RC oscillators.

	LC oscillator	RC oscillator
Stand alone	–131 dBc/Hz	–113 dBc/Hz
Weak coupling	–134 dBc/Hz	–116 dBc/Hz
Strong coupling	–123 dBc/Hz	–123 dBc/Hz

5.5.3 Comparison of measurement results between a 5 GHz CMOS LC oscillator and RC coupled oscillators

5.5.3.1 LC and RC oscillator circuit design

The quadrature LC and RC oscillator schematics shown in Figure 5-5 and Figure 5-10 were implemented in TSMC 0.18 μm process. The NMOS transistor sizes were chosen in order to guarantee start-up conditions and to minimize phase noise. Transistors with a minimum available channel length were chosen in order to minimize parasitic capacitances and allow quadrature operation at 5 GHz. The differential stage transistor sizes were designed to have good quadrature phase accuracy over a large coupling strength range. Spectre RF simulators were used in the design process in order to obtain optimum transistor sizes for minimum phase noise while achieving quadrature outputs. Transistor dimensions of the LC oscillator are: for M transistors, (W/L) = (15*5) μm/0.18 μm, and for M_{SL}, (W/L) = (15*5) μm/0.18 μm. Transistor dimensions of the RC oscillator are: for M transistors, (W/L) = (15*5) μm/0.18 μm, and for M_{SL}, (W/L) = (20*5) μm/0.18 μm. The buffer stage shown in Figure 5-13 was added to the quadrature RC and LC oscillators' output in order to allow each oscillator to drive the 50 ohms measurement system. The stage is composed of a common drain NMOS transistor, bias is provided by a current mirror formed by M_1 and M_2. The circuit parameters are: M_1 = 10 μm/0.5 μm, M_2 = (5*8) μm/0.5 μm, and M_3 = (5*10) μm/0.5 μm. The buffer stage adds 150 fF to each LC tank circuit. To reduce quadrature phase errors caused by mismatch between the two coupled oscillator cores, special care was taken during the layout stage in order to preserve symmetry. Multiple-fingers were used for the layout of transistor gates in order to reduce gate resistance.

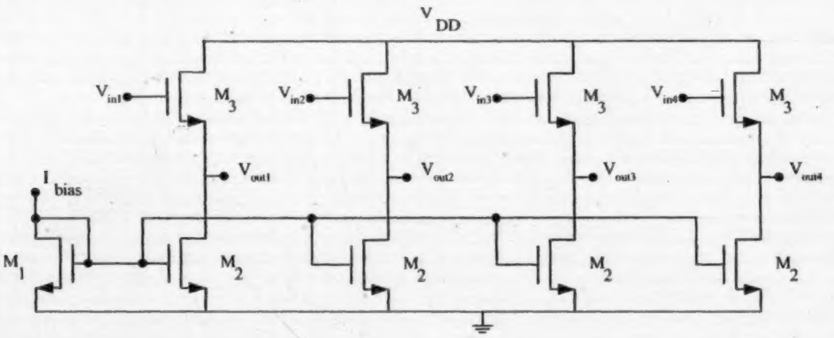


Figure 5-13: LC and RC oscillator buffer.

The integrated inductors were designed on the AlCu thick metal layer of a six-metal layers process. The thickness of each layer is 2.34 μm and has a sheet resistance of 36 mohms/square. The inductors have 3.5 turns, metal strip thickness is 10 μm, the distance between two metal strips is 1.8 μm, and the inductors occupy an area of 150 μm * 150 μm. The inductors achieved a value of 2 nH and a quality factor of 5 at 5 GHz. The metal width and spacing of the integrated inductors were optimised using ASITIC [100] to produce a maximum quality factor at 5 GHz. The resistance and inductance of the metal strips connecting the inductor to the oscillator core slightly reduce the inductor quality factor. The resistors for the RC oscillators were implemented as N+ diffusion resistors. The resistivity of an N+ diffusion layer is 59 ohms/square. The width and number of contacts of each resistor were optimised according to the final values of the bias current of each oscillator. Dummy resistors were added around each section of the original resistor in order to reduce the effects of etching on resistor values. Each oscillator included a 75 ohms resistor. The capacitors were implemented with an on-chip MIM (metal-insulator-metal) layer. MIM capacitors are suitable for CMOS RF integrated circuits due to their small area and high quality factor.

The following figure of merit (FOM) have been used in literature to compare the performance of oscillators [105]:

$$FOM = \mathcal{L}(\Delta f_0) + 10\log\left(\left(\frac{\Delta f_0}{f}\right)^2 \frac{P_{DC}}{P_{ref}}\right) \tag{5.20}$$

Where $\mathcal{L}(\Delta f_0)$ is the phase noise at an offset frequency Δf_0 from the oscillator operating frequency f_0, P_{DC} is the power consumed by the oscillator and P_{ref} is a reference power level (1 mW). A higher negative value of the FOM indicated a better performing oscillator. The comparison results of the performance of the LC quadrature oscillator designed in this thesis recently published quadrature oscillator is shown in Table 5-3.

Table 5-3: Comparison of Quadrature LC oscillators.

Reference	**f_0 [GHz]**	**Phase noise [dBc/Hz]**	**Δf [MHz]**	**P_{DC} [mW]**	**FOM**
[110]	1.88-1.98	-122	0.6	27	-178
[112]	1.77-1.99	-143	3	20	-185
[116]	4.91-5.23	-107	1	21	-168
This work	5	-101	1	5.4	-168

The comparison results shown in Table 5-3, indicate that the quadrature oscillator designed in this thesis have a FOM comparable to quadrature oscillators reported in literature.

5.5.3.2 Measurement results

A die photograph of the 5 GHz LC and RC oscillators is shown in Figure 5-14. The LC quadrature oscillator occupies a die area of 1000 μm by 1000 μm. The core quadrature oscillator draws 1 mA current from a 1.8 V supply. The buffer stage draws 2 mA from a 1.8 V supply. Each section of the oscillator was powered from a different power supply in order to compare the measurements of stand-alone and coupled oscillators. The core RC oscillator occupies a die area of 500 μm by 1000 μm. The added (ground-signal-ground) pad configuration increased the final RC oscillator area to 1000 μm by 1000 μm. Excluding the pads area, the LC oscillator occupies an area of approximately 0.4 mm^2 and the RC oscillator occupies and area of 0.2 mm^2. The core RC oscillator draws 5 mA from a 3 V supply. The output of the oscillator was measured using G-S-G probes. Measurements were taken at room temperature. Quadrature signals from the RC oscillator and the LC oscillator are shown in Figure 5-15 and Figure 5-16. The LC oscillator has a quadrature output of 43 mVpp at 5 GHz. The RC oscillator has a quadrature output of 45 mVpp at 5 GHz. The measurements were done using an HP 54120B digitizing scope. Losses in the coaxial cables and dc blocks connecting the on-wafer probes to the scope were around 7 dB at 5 GHz. With losses included, the actual outputs from each oscillator would be close to 100 mVpp.

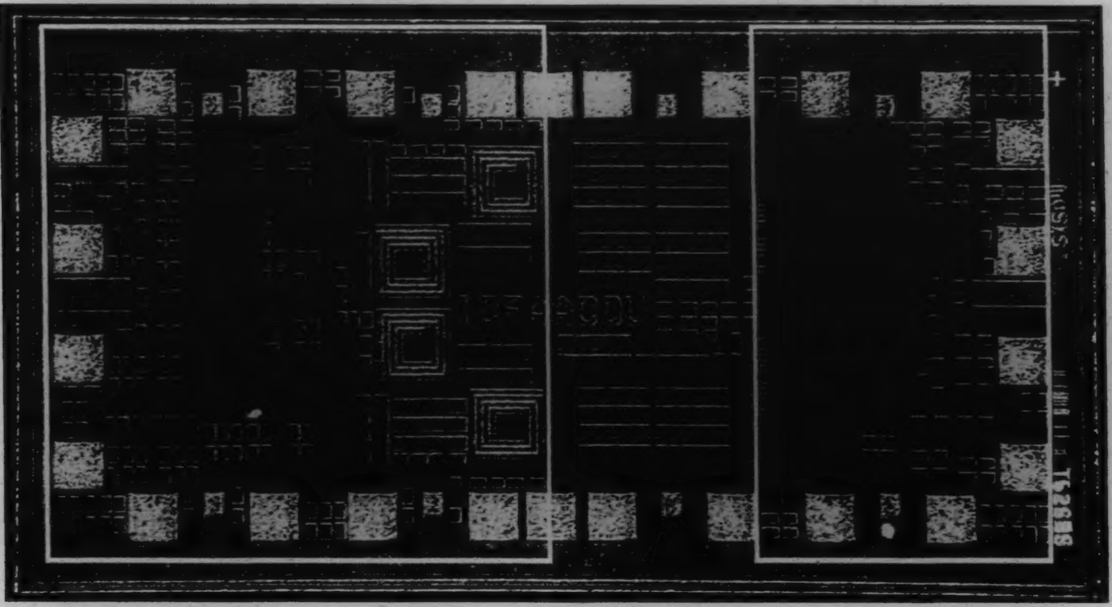
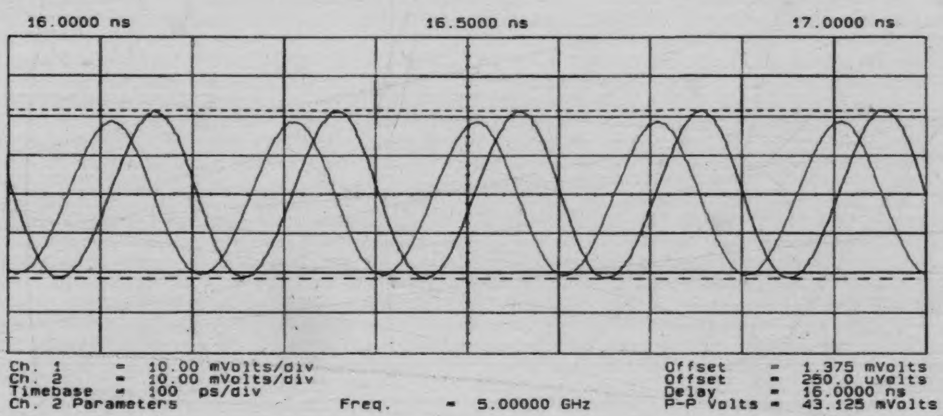
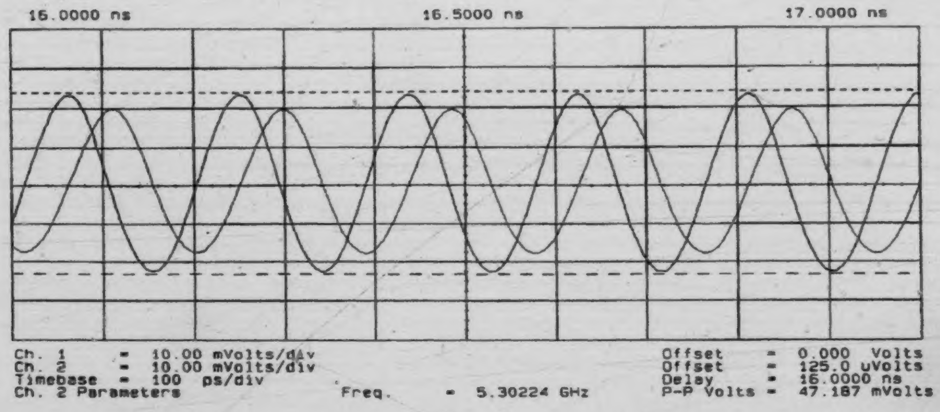

LC Coupled oscillator
RC coupled oscillator

Figure 5-14: Die photograph of RC and LC coupled oscillators. The die dimensions are 1000 µm × 2000 µm including the bond pads.



```
Ch. 1      =  10.00 mVolts/div                          Offset     =  1.375 mVolts
Ch. 2      =  10.00 mVolts/div                          Offset     =  250.0 uVolts
Timebase   =  100  ps/div                               Delay      =  16.0000 ns
Ch. 2 Parameters           Freq.     =  5.00000 GHz     P-P Volts  =  43.125 mVolts
```

Figure 5-15: Measured quadrature LC oscillator output.



```
Ch. 1      =  10.00 mVolts/div                         Offset     =  0.000  Volts
Ch. 2      =  10.00 mVolts/div                         Offset     =  125.0 uVolts
Timebase   =  100  ps/div                              Delay      =  16.0000 ns
Ch. 2 Parameters         Freq.      =  5.30224 GHz     P-P Volts  =  47.187 mVolts
```

Figure 5-16: Measured RC quadrature oscillator output.

Phase noise and spectral measurements were done using the phase noise measurement capability of the HP 71000 spectrum analyzer. Phase noise measurements using a spectrum analyzer produces reasonable results compared to a dedicated phase noise measurement system. In addition, the main objective of the current design was to measure the relative improvement of phase noise while increasing the coupling strength. Absolute phase noise values were of secondary importance in the current study. Results for the measured phase noise and the simulated phase noise using Spectre RF are shown in Table 5-4.

Table 5-4: Phase-noise (@1MHz offset) of the RC and LC oscillators.

	Phase Noise (dBc/Hz)			
	RC oscillator		**LC oscillator**	
	Simulated	**Measured**	**Simulated**	**Measured**
Weak coupling $I_{SL} = 0.5$ mA	-90	-87	-101	-101
Strong coupling $I_{SL} = 3$ mA	-98	-97	-92	-96

Quadrature accuracy was measured using the starting edge detection capability of the HP54120B digitizing oscilloscope. Once the locations of the starting edge of each of the two quadrature signals is determined, the quadrature error can be calculated by comparing the time difference of the two edges to the total signal period. The measured effects of coupling strength on quadrature accuracy and frequency shift of the LC oscillator are shown in Figure 5-17. For LC oscillators, increased coupling reduced the quadrature error from 3.5° to 1.5°. However, the phase noise was reduced by 7 dB. Compared to the stand-alone oscillator, coupling increased phase noise. For RC oscillators, increasing coupling strength reduced quadrature error from 2.7° to 1°. The phase noise was improved by more than 8 dB. With increased coupling strength, RC oscillators showed a phase noise and quadrature error performance similar to LC oscillators. The variation in frequency with coupling in LC oscillators depends on the method of coupling as discussed in section 5.4.1. Unlike LC oscillators, coupling in RC oscillators can be realized without a frequency shift in the operating frequency.

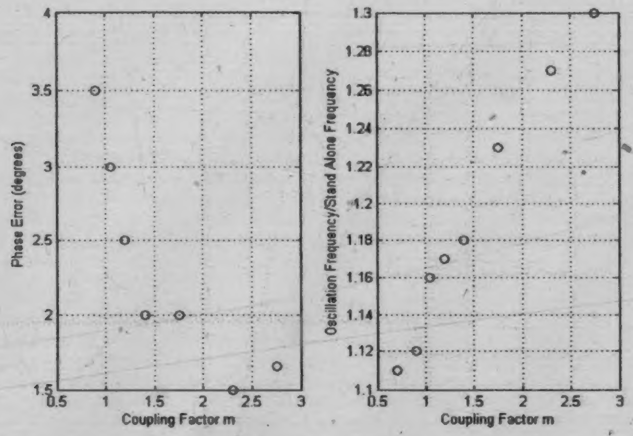


Figure 5-17: LC oscillator phase error and frequency deviation.

5.6 Conclusion

Various methods of generating quadrature signals using LC oscillators were reviewed. Quadrature oscillators can be realized using odd or even harmonic coupling. The coupling network acting on the odd or even harmonics can be realized using active or passive devices.

Two LC oscillators, cross-coupled for synchronized operation, are widely used for quadrature generation. In this chapter, an analysis of the amplitude and frequency of oscillation for two van der Pol oscillators is presented. Theoretical analysis indicated that the synchronization frequency will be different from the frequency of each oscillator, and, in general the amplitudes will be different.

Relaxation oscillators can be used to generate quadrature signals. However, their phase noise performance is worse than the phase noise of LC oscillators. A block diagram of the influence of noise sources on RC oscillator outputs indicates that with a high coupling gain, the input noise signal is attenuated by the feedback. RC and LC oscillators were compared for effects of coupling strength on phase noise and quadrature error. Measurements on 5 GHz CMOS oscillators indicate that RC and LC quadrature oscillators are affected by coupling strength differently. Stronger coupling simultaneously improves the quadrature relationship and phase noise performance in RC oscillators. Increasing coupling to obtain a better quadrature relationship worsens the phase noise performance in LC oscillators. Quadrature relaxation oscillators might be considered an alternative to quadrature LC oscillators in applications that require die area minimization (as inductors are omitted from the design).

Chapter 6

Summary and Conclusions

6.1 Thesis summary

The motivation for the current work was the need to improve the performance of quadrature oscillators designed in CMOS technology. Achieving this task entailed an understanding of the various mechanisms affecting significant oscillator parameters such as phase noise and quadrature accuracy. A comprehensive study of MOSFET noise modeling and quadrature signal generation using CMOS LC and RC oscillators is presented.

In Chapter 3, high frequency MOSFET models and noise models were investigated. Several noise models suitable for MOSFETs operating at radio frequencies were compared. NMOS devices with channel widths of 120 μm (20 μm*6 fingers) and channel lengths of 0.18 μm, 0.36 μm, and 0.54 μm were compared. The drain thermal noise was measured over a frequency range of 3 GHz to 6 GHz and a gate overdrive voltage of 0.2 V to 1.2 V. The model proposed by Deen *et al.* [31] for drain thermal noise provided the best match between measured and simulated results for all devices.

Guidelines needed for the design and optimization of VCO phase noise have been reviewed. These guidelines were applied to the design of a 5 GHz quadrature LC oscillator in CMOS 0.18 μm technology. The oscillator was designed using cross-coupled differential topology. Relaxation oscillators can be used to generate quadrature signals, however, their phase noise performance is worse than that of LC oscillators. Measurements on 5 GHz CMOS oscillators indicate that RC and LC quadrature oscillators are affected by coupling strength differently. Stronger coupling simultaneously improves the quadrature relationship and phase noise performance in RC oscillators. Increasing coupling to obtain a better quadrature relationship worsens the phase noise performance in LC oscillators. A relaxation oscillator might be considered an alternative to an LC oscillator in applications that require die area minimization (as inductors are omitted from the design). RC oscillators can also be realized in low cost technology as a thick metal layer is not required. Considering that the current consumption of RC oscillators is higher than that of LC oscillators, high performance can be achieved by spending more power.

6.2 Author's contribution

The topics covered in this thesis contribute to two areas of RF front-end design: noise modeling in RF MOSFETs and quadrature signal generation using RC and LC oscillators.

Comparisons between the predictive capability of several MOSFET RF noise models and experimental results obtained in this study have proved to be a valuable benchmark for the development of future noise models [134]. An extensive model extraction procedure is presented. An automatic tuner based noise parameters measurement system is discussed. Measurements were made on MOSFETs fabricated in TSMC 0.18 μm technology.

The second topic includes a study of quadrature LC and RC oscillators emphasizing frequency, amplitude of oscillation, and phase noise. First, we studied coupled oscillators using ideal blocks, then we proceeded to circuit level. A review of state-of-the-art phase noise models is presented. Results indicate that, with increasing coupling strength, quadrature RC oscillators can be considered as alternatives to quadrature LC oscillators. We confirmed the theoretical proof and simulation results by measurements done on 5 GHz quadrature RC and LC oscillators built in TSMC 0.18 μm technology [126], [135].

The development of quadrature mutually coupled LC oscillators is limited by an effort to stay in the frame of linear theory. However, a full explanation of synchronization can be obtained only by referring to nonlinear theory, as synchronization is a deeply nonlinear phenomenon. We present a theoretical model, which predicts amplitude and frequency of oscillation of two coupled van der Pol oscillators [126].

The topics studied over the period of this research led to contributions in the area of RF front-end design, including the design of a new configuration for a CMOS two-stage wideband amplifier [136] and a new CMOS wideband RF front-end for multistandard low-IF wireless receivers [137]. Novel architectures for CMOS voltage references suitable for low voltage operation were presented in [138], [139]. However, these contributions are outside the scope of this thesis.

- A. Allam, and I. M. Filanovsky, "High frequency channel noise measurement and characterization in deep submicron MOSFETs," *J. Analog Integrated Circuits and signal Processing,* submitted.

- L. B. Oliveira, A. Allam, I. M. Filanovsky, J. Fernandes, C. Verhoeven, and M. M. Silva, "Quadrature Error and Phase-Noise of Cross-Coupled RC and LC oscillators," *IEEE Transactions on Circuits and Systems*, *Part II*, to be submitted.
- A. Allam, and I. M. Filanovsky, "High Frequency Channel Noise Measurement and Characterization in Deep Submicron MOSFETs," in *Proc. Midwest Symposium on Circuits and Systems*, 2007, pp. 1348–1351. Selected as one of 10 finalists at the student paper contest.
- A. Allam, and I. M. Filanovsky, "Experimental comparison of coupling effects on the performance of quadrature CMOS LC and RC oscillators," in *Proc. Midwest Symposium on Circuits and Systems*, 2007, pp. 606–609.
- A. Allam, I. M. Filanovsky, L. B. Oliveira, and J. R. Fernandes, "Synchronization of mutually coupled LC-oscillators," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2006, pp. 4297–4300.
- I. M. Filanovsky, A. Allam, L. B. Oliveira, and G. R. Fernandes, "Quadrature van der Pol oscillators using second harmonic coupling," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2006, pp. 1663–1666.
- I. M. Filanovsky, A. Allam, L. B. Oliveira, and G. R. Fernandes, "Synchronization of van der Pol oscillator by external voltage of doubled frequency," *Midwest Symp. Circuits and Systems*, vol. 1, 2006, pp. 56–59.
- L. B. Oliveira, A. Allam, I. M. Filanovsky, and J. R. Fernandes, "On phase noise in quadrature cross-coupled oscillators," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2005, pp. 2635–2638.
- I. M. Filanovsky, M. M. Reja and A. Allam, "A new configuration of CMOS two-stage wide-band amplifier," in *Proc. IEEE Int. Midwest Symposium on Circuits and Systems*, vol. 3, 2004, pp. 13–16.
- M. M. Reja, A. Allam, and I. M. Filanovsky, "A new CMOS wideband RF front-end for multistandard low-IF wireless receivers," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 3, 2005, pp. 2120–2123.
- I. M. Filanovsky, F. Fang, A. Allam, and Kris Iniewski, "0.6 V supply voltage references for CMOS technology based on threshold-voltage difference architecture," in *Proc. IEEE Int. Midwest Symposium on Circuits and Systems*, vol. 2, 2005, pp. 1790–1793.
- I. M. Filanovsky, V. Ivanov, F. Fang, and A. Allam, "Sub 1-V Supply CMOS voltage reference based on asymmetric differential stage with feedback," in *Proc. IEEE Int. Midwest Symposium on Circuits and Systems*, vol. 1, 2006, pp. 127–130.

6.3 Recommendations for further studies

The work presented in this thesis suggests opportunities for further research. Recommendations for future projects are outlined in this section.

RF building blocks implemented in current CMOS technology and having performance comparable to RF circuits built in other semiconductor technologies have been reported. Although RF noise models for current CMOS technologies were presented in this thesis, further research is needed to study the effects of downscaling on CMOS RF noise performance [31]. An important issue of future work is the study of shot noise due to gate tunneling and its correlation to drain and gate noise sources. In the current noise models, parasitic resistances surrounding the MOSFETs were assumed to be bias independent. Noise generated due to bias dependence of the parasitic resistances needs to be modeled [31].

The focus of this thesis was modeling and measurement of noise sources in linear RF building blocks. A linear noisy two-port can be represented by a linear noiseless two-port driven by two hypothetical noise sources. In addition, measurement techniques for noise parameters for a linear two port have been demonstrated. In nonlinear RF circuits such as oscillators and mixers, noise frequency conversion plays a significant role. A unified method of modeling noise sources of devices operating nonlinearly is absent. More work is needed to study modeling of noise sources, measurement techniques, and frequency conversion mechanisms in RF circuits operating in the nonlinear regime. Optimizing noise performance of nonlinear RF circuits is an ongoing goal. A setup for nonlinear noise measurement was demonstrated in [67].

In this thesis we proposed quadrature RC oscillators as potential candidates for quadrature LC oscillators in modern RF transceivers. RC oscillators have the advantage of reduced area compared to LC oscillators. In addition, RC oscillators can be integrated in standard CMOS processes. However, a drawback of RC oscillators is high power consumption. A future research topic, would be to investigate design methodologies to reduce power consumption of RC oscillators.

The LC oscillators compared in this thesis were coupled using the first harmonic. In this type of coupled oscillators, phase noise was increased with increasing quadrature power. Effects on phase noise of other methods of coupling (for instance second harmonic coupling) is an important topic for future research.

The inductors used in the LC coupled oscillators shown in Figure 5-5, were designed using square spiral structures due to the limitations of ASITIC. A future project could investigate the area saving and phase noise improvement introduced by designing LC coupled oscillators using center-tapped inductors.

The current study did not include estimates of the effects of varactors on coupled LC oscillators' phase noise performance. The effects of varactors on coupled LC oscillator phase noise could be studied and compared with varactor effects on coupled RC oscillators with similar tuning ranges.

The inductor value required for an LC oscillator is reduced as the frequency of operation is increased. A future topic would consider the reduction in inductor size in a coupled high frequency oscillator while comparing coupled RC oscillators operating at the same frequency.

Phase noise theory of stand-alone oscillators has been extensively studied. This wealth of literature does not exist for coupled oscillators. A mathematical theory is needed to study the effects of coupling strength on phase noise and quadrature error in coupled oscillators.

Appendix A

CMOS Voltage Controlled Oscillator

A.1 Introduction

This appendix summarizes the design procedure of a negative resistance oscillator using a complementary topology in conjunction with PMOS varactors to realize a fully integrated VCO. The schematic of the oscillator is shown in Figure 4-6. There are several reasons for the superiority of the complementary structure over the all-NMOS structure. The complementary structure offers higher transconductance for a given current, which results in faster switching of the cross-coupled differential pair. This structure also offers better rise- and fall-time symmetry, which results in less up-conversion of flicker noise and other low frequency noise sources [97]–[140]. The selection of a differential oscillator topology imposes some design constraints on inductor and varactor selection as will be shown in sections A.2 and A.3.

A.2 Inductor selection

A simplified expression of the LC oscillator phase noise can be given by [8]:

$$\mathcal{L}(\Delta\omega) = 10.\log\left\{\frac{2KT}{P_{sig}}\left[\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\right\}, \tag{A.1}$$

where $\mathcal{L}(\omega)$ is the oscillator phase noise at an offset frequency of $\Delta\omega$ from a carrier frequency ω_o, P_{sig} is the carrier power, and Q is the tank circuit quality factor. The oscillator operating frequency is given by:

$$\omega_0 = \sqrt{LCeq}\ . \tag{A.2}$$

where L and C_{eq} are the equivalent inductance and capacitance of the parallel tank circuit. The impedance of the tank at resonance is equal to R_p, and can be given by:

$$R_p = \frac{(L\omega_0)^2}{R_s}\ . \tag{A.3}$$

where R_s is a series resistance that models the loss of the inductor. A large inductance value is desired in order to maximize the equivalent parallel resistance of the tank. Increasing this resistance lowers the power consumption since the transconductances required to start the oscillator become smaller. In addition to the loss of die area, maximizing the value of the inductor entails two trade-offs. First, the self-resonance frequency of the inductor decreases, approaching the oscillation frequency of interest. Second, the tank capacitance becomes limited by the inductor parasitic capacitances, making it difficult to vary the frequency by adding a variable capacitor to the oscillator. Thus, a compromise in selection of the inductor size is usually necessary.

A.3 Varactor selection

The tunable element of the VCO is implemented using a PMOS varactor [99]. Although the varactor contribution to the VCO total phase noise is low, PMOS varactors were shown to introduce lower phase noise than their NMOS counterparts [99]. The PMOS varactors' capacitances combined with the VCO active elements parasitic capacitances form the total tank capacitance. Two of these PMOS varactors are connected in series to preserve symmetry. The tuning voltage is supplied at the common drain-source node.

A.4 Experimental results

The above guidelines were used in the design of a VCO using TSMC 0.18 μm technology. The oscillator layout is shown in Figure A.1. The die photograph of the oscillator is shown in Figure A.2. The VCO operates from a 1.8 V supply and the oscillator core consumes 5 mA of current. Including the on-chip inductors, the oscillator occupies an area of 900 μm by 500 μm including the pond pads. The total die area is 2300 μm by 1700 μm. The die includes transformer test structures that were not covered in this thesis. The VCO output at 900 MHz is shown in Figure A.3. Phase noise at 600 kHz from the 900 MHz carrier was measured to be –82 dBc/Hz as shown in Figure A.4. With a control voltage ranging from 0.5 V to 1.8 V the VCO was able to oscillate from 850 MHz to 900 MHz. The tuning characteristics of the VCO are shown in Figure A.5.

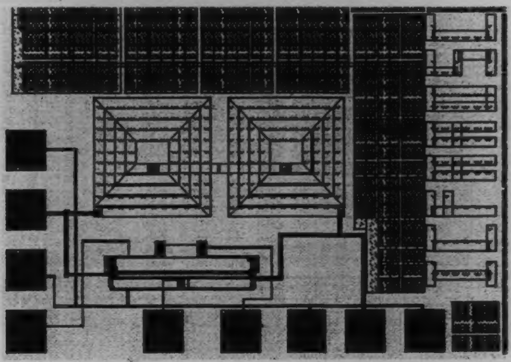


Figure A.1: Oscillator layout.

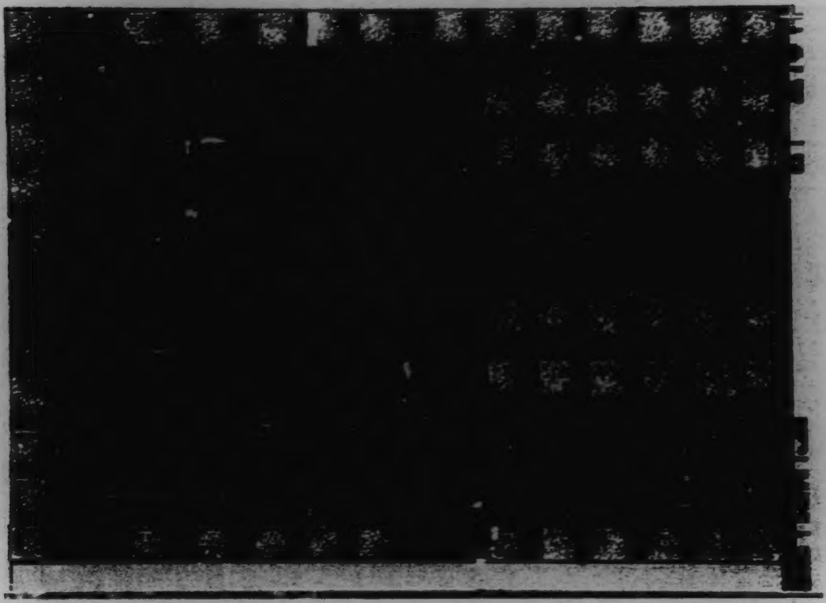


Figure A.2: Oscillator die photograph including test structures. The oscillator dimensions are 2300 μm × 1700 μm.

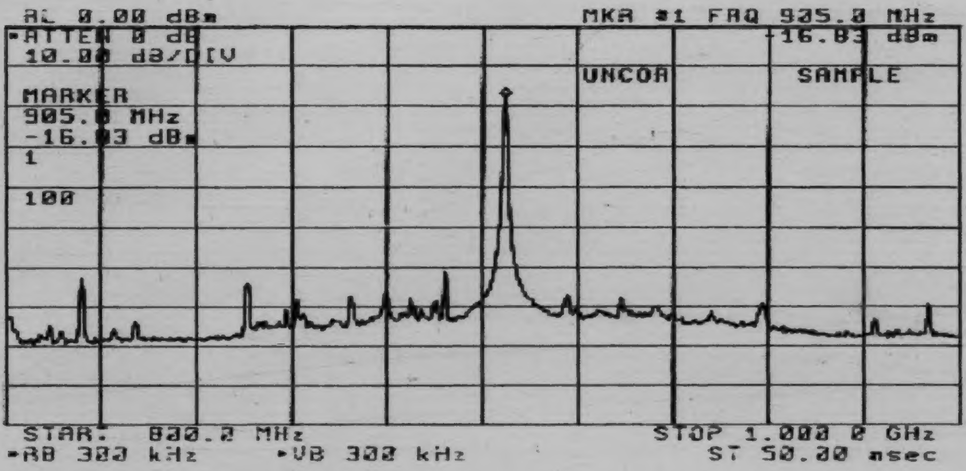


Figure A.3: Oscillator output at 900 MHz.

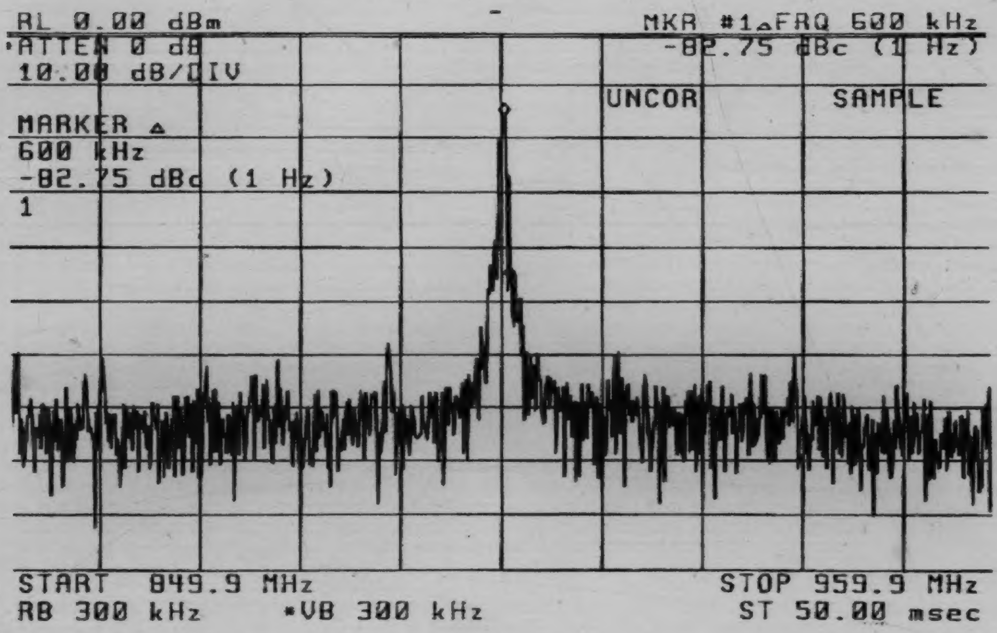


Figure A.4: Oscillator phase noise at 600 kHz from the 900 MHz carrier.

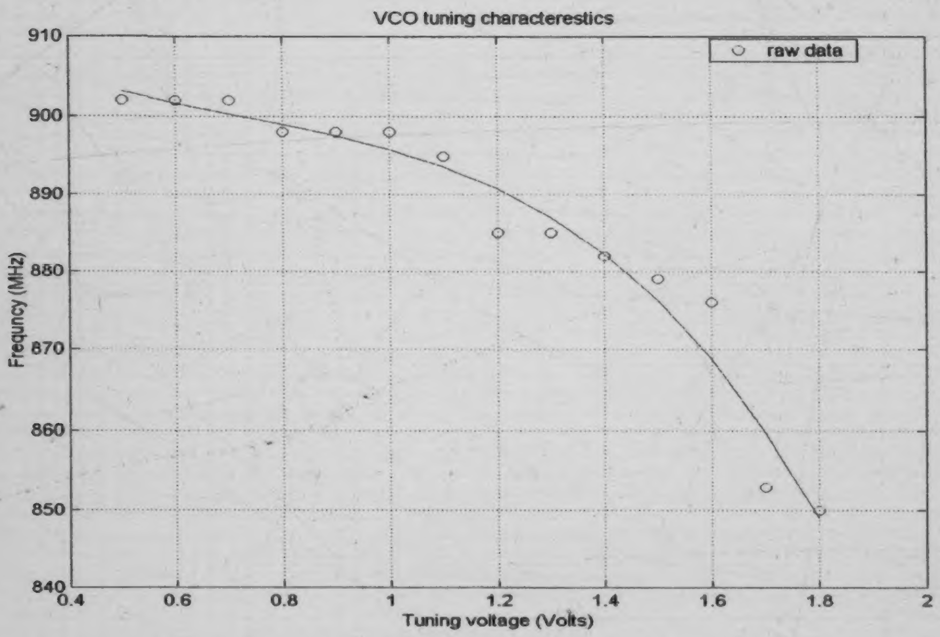


Figure A.4: Oscillator tuning characteristics.

Bibliography

[1] A. Abidi, "RF CMOS comes of age," *IEEE J. Solid State Circuits*, vol. 39, no. 4, pp. 549–561, April 2004.

[2] T. Lee and S. Wong, "CMOS RF integrated circuits at 5 GHz and beyond," *Proc. IEEE*, vol. 88, no. 10, pp. 1560–1571, October 2000.

[3] J. Sevenhans, F. Eynde, and P. Reusenss, "The silicon radio decade," *IEEE Transactions on Microwave Theory and Technique*, vol. 50, no. 1, pp. 235–244, January 2002.

[4] A. Springer, and R. Weigel, "RF microelectronics for W-CDMA mobile communications systems," *Electronics and Communications Engineering Journal*, vol. 14, no. 3, pp. 92–100, June 2002.

[5] M. Feng, S. Shen, D. Caruth and J. Huang, "Device technologies for RF front-end circuits in next-generation wireless communications," *Proc. IEEE*, vol. 92, no. 2, pp. 354–375, February 2004.

[6] A. Joseph, D. L. Harame, B. Jagannathan, D. Coolbaugh, D. Ahlgren, J. Magerlein, L. Lanzerotti, N. Feilchenfeld, S. St Onge, J. Dunn, E. Nowak, "Status and direction of communication technologies-SiGe, BiCMOS and RFCMOS," *Proc. IEEE*, vol. 93, no. 9, pp. 1539–1558, September 2005.

[7] B. Razavi, *RF Microelectronic*. Prentice Hall, 1998.

[8] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 1998.

[9] K. McClaning, and T. Vito, *Radio Receiver Design*, Nobel Publishing Corporation, 2000.

[10] A. Rofougaran, M. Rofougaran and A. Behzad, "Radios for next-generation wireless networks," *IEEE Microwave Magazine*, vol. 6, no. 1, pp. 38–43, March 2005.

[11] P. B. Kenington, *RF and Baseband Techniques for Software Defined Radio*. Artech House, Inc. 2005.

[12] M. Steyaert, "Single chip CMOS RF circuits: Wishful thinking or reality?," 1st *IEEE-CAS Workshop on Wireless-Communication Circuits and Systems*, June 22–24, Lucerne, Switzerland, 1998.

[13] C.-H. Chen, "Issues in high-frequency noise characterization and modeling of MOSFETS," in *Proc. IEEE International Workshop on Radio-Frequency Integration Technology*, 2005, pp. 119–122.

[14] S. Jen, C. Enz, D. Pehlke, M. Schroter, and B. Sheu, "Accurate modeling and parameter extraction for MOS transistors valid up to 10 GHz," *IEEE Transactions on Electron Devices*, vol. 46, no. 11, pp. 2217–2227, November 1999.

[15] D. Lovelace, J. Costa, and N. Camilleri, "Extracting small-signal model parameters of silicon MOSFET transistors," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, 1994, pp. 865–868.

[16] Y. Khallaf, "Systematic Optimization Techniques for MESFET Modeling". Ph. D. dissertation, Virginia Polytechnic Institute and State University, July 2000.

[17] T. Ytterdal, Y Cheng, and T. Fjeldly, *Device Modeling for Analog and RF CMOS Circuit Design*. John Wiley and Sons, Ltd., 2003.

[18] W. Liu, R. Gharpurey, M. C. Chang, U. Erdogan, R. Aggarwal, and J. P. Mattia, "RF MOSFET modeling accounting for distributed substrate and channel resistance with emphasis on the BSIM3V3 SPICE model," in *Technical Digest International Electron Devices Meeting*, 1997, pp. 309–312.

[19] Y. Cheng, and M. Matloubian, "On the high frequency characteristics of the substrate resistance in RF MOSFETs," *IEEE Electron Device Letters*, vol. 21, no. 12, pp. 604–606, 2000.

[20] J.-J. Ou, X. Jin, I. Ma, C. Hu and P. Gray, "CMOS RF modeling for GHz communications IC's," in *Proceedings of the VLSI Symposium on Technology*, 1998, pp. 94–95.

[21] A. Van der Ziel, "History of noise research," *Advances in Electronics and Electron Physics*, vol. 50, 1980, pp. 351–409.

[22] Haus and Adler, *Circuit theory of linear noisy networks*. John Wiley, 1959.

[23] H. Rothe, and W. Dahlke, "Theory of noisy four poles," *Proc. of the IRE*, vol. 44, pp. 811–818, 1956.

[24] G. D. Vendelin, A. Pavio, and U. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques*. John Wiley and Sons, Ltd., 2005.

[25] A. Lyoubi, "Métrologie et modélisation du bruit basse fréquence dans les transistors à effet de champ: application à la CAO des sources dans les systèmes de communication" Ph.D. dissertation, Université de Limoges, France, 2002.

[26] A. Ambrozy, *Electronic Noise*. McGraw-Hill, 1980.

[27] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*. Prentice Hall, 1996.

[28] W. Grabinski, B. Nauwelaers, and D. Schreurs, *Transistor level modeling for Analog/RF IC Design*. Springer, 2006.

[29] A. Van der Ziel, "Thermal noise in field-effect transistors," *Proc. of the IRE*, vol. 50, 1962.

[30] A. Abidi, "High frequency noise measurements on FETS with small dimensions," *IEEE Transactions on Electron Devices*, vol. ED-33, no. 11, pp. 1801–1805, November 1986.

[31] M. J. Deen, C.-H. Chen, S. Asgaran, G. Rezgani, J. Tao, and Y. Kiyota, "High frequency noise of modern MOSFETs: Compact modeling and measurement issues," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 2062–2081, September 2006.

[32] C.-H. Chen, and M. J. Deen, "Channel noise modeling of deep submicron MOSFET," *IEEE Transactions on Electron Devices*, vol. 49, no. 8, pp. 1484–1487, August 2002.

[33] A. J. Scholten, A.J.; L. F. Tiemeijer, R. van Langevelde, R. J. Havens, R.J.; A. Zegers-van Duijnhoven, and V. C. Venezia, "Noise modeling for RF CMOS circuit simulation," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 618–632, March 2003.

[34] D. Greenberg, "Evolving and emerging challenges in the modeling of RF noise in FETs," *Workshop, International Microwave Symposium*, 2006.

[35] C.-H. Chen, "Noise characterization and modeling of MOSFETs for RF IC applications" Ph.D. dissertation, McMaster University, September 2002.

[36] G. Knoblinger, P. Klein, and M. Tiebout, "A new model for thermal channel noise of deep submicron MOSFETS and its application in RF CMOS design," *IEEE J. of Solid State Circuits*, vol. 36, no. 5, pp. 831–837, May 2001.

[37] R. Kraus, and G. Knoblinger, "Modeling the gate-related high-frequency noise and noise Characteristics of deep-submicron MOSFETs," in *Proc. IEEE Custom Integrated Circuit Conference,* 2002, pp. 209–212.

[38] Van der Ziel, "Gate noise in field-effect transistors at moderately high frequency," *Proc. IEEE*, vol. 51, no. 3, pp. 461–467, March 1963.

[39] F. M. Klaassen, "High frequency noise of the junction field-effect transistor," *IEEE Transactions on Electron Devices*, vol. 14, no. 7, pp. 368–373, July 1967.

[40] S. Lee, K. Webb, V. Tilak, and L. Eastman, "Intrinsic noise equivalent-circuit parameters for AlGan/Gan HEMTS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 5, pp. 1567–1577, May 2003.

[41] D. Shaeffer, and T. Lee, "A 1.5 V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.

[42] D. Shaeffer, and T. Lee, "Corrections to: A 1.5 V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1397–1398, June 2005.

[43] W. Wu, S. Lam, and M. Chan, "Effects of layout methods of RF CMOS on noise performance," *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2753–2759, December 2005.

[44] R. P. Jindal, "Distributed substrate resistance noise in fine line NMOS field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 32, no. 6, pp. 1047–1052, June 1985.

[45] R. Pucel, W. Struble, R. Hallgren, and U. Rhode, "A general noise deembedding procedure for packaged two-port linear active devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 11, pp. 2013–2024, November 1992.

[46] R. Q. Lane, "The determination of device noise parameters," *Proc. IEEE*, vol. 57, no. 8, pp. 1461–1462, 1969.

[47] Maury Microwave Corporation, "http://www.maurymw.com"

[48] D. Pasquet, *Mesures en Hyperfréquences*. Lavoisier, 2004.

[49] S. Van Den Bosch, and L. Martens, "Improved impedance pattern generation for automatic noise parameter measurements," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 11, pp. 1673–1678, November 1998.

[50] A. Boudiaf, and M. Laporte, "An accurate and repeatable technique for noise parameter measurements," *IEEE Transactions on Instrumentation and Measurement*, vol. 42, no. 2, pp. 532–537, April 1993.

[51] G. Vasilescu, G. Alquie, and M. Krim, "Exact computation of two-port noise parameters," *Electronics Letters*, vol. 25, no. 4, pp. 292–293, February 1989.

[52] L. Escotte, R. Plana, and J. Garffeuil, "Evaluation of noise parameter extraction methods," *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, no. 3, pp. 382–387, March 1993.

[53] L. F. Tiemeijer, R. J. Havens, R. de Kort, and A. J. Scholten, "Improved Y-Factor method for wide-band on-wafer noise parameter measurements," *IEEE Transactions Microwave Theory and Techniques*, vol. 53, no. 9, pp. 2917–2925, September 2005.

[54] "Layout rules for GHz-probing," Cascade Microtech, Application Note, 1998.

[55] M. J. Deen, and C.-H. Chen, "The impact of noise parameters deembeding on high frequency noise modeling of MOSFETs," in *Proc. IEEE International Conference on Microelectronic Test Structures*, March 1999, pp. 34–39.

[56] M. Yang, P. Ho, Y. Wang, T. Yeh, and Y. Chia, "Broad band small-signal model and parameter extraction for deep sub-micron MOSFETs valid up to 110 GHz," *IEEE Radio Frequency Integrated Circuits Symposium Digest, 2003,* pp. 369–372.

[57] A. Grebennikov, *RF and Microwave Power Amplifier Design*. McGraw Hill, 2005.

[58] S. Wartenberg, *RF Measurements of DIE and Packages*. Artech House, 2002.

[59] U. Rohde, A. K. Poddar, and G. Bock, *The Design of Modern Microwave Oscillators for Wireless Applications.* John Wiley and Sons, Inc., 2005.

[60] D. B. Leeson, "A simple model of feed back oscillator noise spectrum," *Proc. IEEE*, vol. 54, no. 2, pp. 329–330, 1966.

[61] A. Demir, A. Mahrota, and J. Roychowdhury, "Phase noise in oscillators: a unifying and numerical method for characterization," *IEEE Transaction Circuits and Systems I: Fundamental Theory and Applications*, vol. 47, no. 5, pp. 655–673, May 2000.

[62] A. Mahrota, and A. Sangiovanni-Vincentelli, *Noise Analysis of Radio Frequency Circuits*. Kluwer Academic Publishers, 2004

[63] G. Braun, and H. Lindenmeier, "Transistors oscillators with impedance noise matching," *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 9, pp. 1602–1610, September 1991.

[64] H. Lindenmeier, "Noise matching techniques in transistor oscillators," in *Proc. IEEE Int. Symp. Circuits and Systems*, 1980, pp. 1052–1055.

[65] J. Everard, *Fundamentals of RF Circuit Design with Low Noise Oscillators*. 2001 John Wiley & Sons, Ltd.

[66] J. Everard, and M. A. Page-Jones, "Ultra low noise microwave oscillators with low residual flicker noise," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, 1995, pp. 693–696.

[67] O. Llopis and G. Cibiel, "Phase noise metrology and modeling of microwave transistors applications to the design of state of the art Dielectric Resonator Oscillators," *Fluctuations and Noise conference*, 2003, pp. 179–191.

[68] M. Regis, H. Lafontaine, S. Kovacic, G. Cibiel, and O. Llopis, "Design of a low phase noise ku-band oscillator using a SiGe HBT," *Microwave Journal*, pp. 136–146, October 2001.

[69] E. Vaury, V. Giordano, J. C. Nallatamby, J. Groslambert, N. Camiade, N. Prigent, O. Llopis, E. Gonzalez, N. Chaubet, and J. Obregon, "A new design method for the design of ultra low noise oscillator," in *Proc. Joint Meeting of the European Frequency and Time Forum and the IEEE International Frequency Control Symposium,* vol. 2, April 1999, pp. 557–560.

[70] A. Von Staveren, and C. J. M Verhoeven, "Optimizing a resonator tap for maximizing oscillator carrier-to-noise ratio," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2001, pp. 480–483.

[71] A. Hajimiri, and T. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, February 1998.

[72] A. Hajimiri, and T. Lee, "Corrections to: A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 6, pp. 928, June 1998.

[73] S. Magierowski, and S. Zukotynski, "Nonlinear analysis of CMOS LC-tuned VCO phase noise," in *Proc. IEEE Int. Midwest Symposium on Circuits and Systems*, vol. 1, 2002, pp. 5–8.

[74] E. Hegazi, Jacob Rael and A. Abidi, *High-Purity Oscillators*. Kluwer Academic Publisher, 2005.

[75] D. Cordeau, J. M. Paillot, C. Duvanaud and L. Dascalescu, "Méthode de recherche de l'optimum de bruit de phase dans les oscillateurs LC - Applications," *13emes Journées Nationales Microondes*, 2003, pp. 582.

[76] T. Song and E. Yoon, "A 1-V 5 GHz low phase noise LC-VCO using voltage-dividing and bias-level shifting technique," in *Topical Meeting on Silicon Monolithic Integrated Circuits in RF systems Digest*, 2004, pp. 87–90.

[77] J. R. Vig (chair.), IEEE Std 1139-1999, IEEE Standard Definitions of Physical Quantities for Fundamental Frequency and Time Metrology-Random Instabilities. IEEE, 1999.

[78] A. Pikovsky, M. Rosenblum, and J. Kurths, *Synchronization, a Universal Concept in Nonlinear Science*. Cambridge University Press, 2001.

[79] D. Ham, and A. Hajimiri, "Virtual damping and Einstein relation in oscillators," *IEEE J. Solid-State Circuits*, vol. 38, no.3, pp. 407–418, March 2003.

[80] S. K. Magierowski, and S. Zukotynski, "CMOS LC-oscillator phase-noise analysis using nonlinear models," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 4, pp. 664–677, April 2004.

[81] B. De Muer, M. Borremans, M. Steyaert, and G. Li. Puma, "A 2-GHz low-phase-noise integrated LC-VCO set with flicker-noise upconversion minimization," *IEEE J. Solid-State Circuits,* vol. 35, no. 7, pp. 1034–1038, July. 2000.

[82] L. Forbes, M. Cheng, and J. Zhou, "Simulation of phase noise generated by white noise in 1.7 GHz CMOS LC oscillator," *Electronics Letters*, volume 36, no. 23, pp. 1909–1911, 9 Nov. 2000.

[83] E. Rubiola, and V. Giordano, "A Low flicker scheme for the real time measurement of phase noise," in *Proc. IEEE International Frequency Control Symposium,* 2001, pp. 138–143.

[84] E. Rubiola, The Leeson Effect—Phase Noise in Quasilinear Oscillators. available at: http://www.femto-st.fr/~rubiola.

[85] L. M. Franco-Neto, R. E. Bishop, and B. A. Bloechel, "64 GHz and 100 GHz VCOs in 90 nm CMOS using optimum pumping method," in *IEEE International Solid-State Circuits Conference Digest,* 2004, pp. 444–445.

[86] B. Jung, and R. Harjani, "A 20 GHz VCO with 5 GHz tuning range in 0.25 μm SiGe BICMOS," in *IEEE International Solid-State Circuits Conference Digest,* 2004, pp. 178–179.

[87] H. Li, H.-M. Rein, T. Suttorp, and J. Bock, "Fully integrated SiGe VCOs with powerful output buffer for 77-GHz automotive radar systems and applications around 100 GHz," *IEEE J. Solid-State Circuits* , vol. 39, no. 10 , pp. 1650–1658, October 2004.

[88] S. W. Yoon, S. Hong, and J. Lasker, "Efficiency enhanced and harmonic suppressed differential VCO with novel buffer scheme using transformers for IEEE 802.11A," IEEE MTT-S *International Microwave Symposium Digest*, vol. 3, 2003, pp. 2181–2184.

[89] M. Steyaert, J. Janssens, B. De.Muer, M. Borremans, and N. Itoh, "A 2-V CMOS cellular tranceiver front end," *IEEE J. Solid State Circuits*, vol. 35, no. 12, pp. 1895–1907, December 2000.

[90] O. Llopis, "Noise in SiGE and III-V HBTs and circuits: opportunities and challenges," *Workshop, International Microwave symposium,* 2006.

[91] R. G. Rogers, *Low Phase Noise Microwave Oscillator Design*. Artech House, Inc. 1991.

[92] T. G. van de. Roer, *Microwave Electronic Devices*. Chapman & Hall, 1994.

[93] L. Dai, and R. Harjani, *Design of High Performance CMOS Voltage Controlled Oscillators*. Kluwer Academic Publishers, 2003.

[94] P. Andreani, S. Mattisson, "A 2.4 GHz CMOS monolithic VCO with an MOS varactor," *Analog Integrated Circuits and Signal Processing,* vol. 22, no. 1, pp. 17–24, January 2000.

[95] M. Rachedine, D. Kaczman, A. Das, M. Shah, J. Mondal, and C. Shurboff, "Performance review of integrated CMOS VCO circuits for wireless communications," in *IEEE Radio Frequency Integrated Circuit Symposium Digest*, 2003, pp. 77–80.

[96] R. Bunch, and S. Raman, "A 0.35 μm CMOS 2.5 GHz complementary $-G_M$ VCO using PMOS inversion model varactors," in *IEEE Radio Frequency Integrated Circuit Symposium Digest*, 2001, pp. 49–52.

[97] D. Ham, and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 896–909, June 2001.

[98] M. del Hershenson, A. Hajimiri, T. H. Lee, "Design and optimization of spiral inductors for Si RF ICs," in *IEEE/ACM International Conference on Computer Aided Design Digest*, 1999, pp. 65–69.

[99] P. Andreani, and S. Mattisson, "On the use of MOS varactor in RF VCOs," *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 905–910, June 2000.

[100] A. M. Niknejad, and R. G. Meyer, "Analysis, design and optimization of spiral inductors for Si RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1470–1481, October 1998.

[101] J. N. Burghartz, M. Soyuer and K. A. Jenkins, "Microwave inductors and capacitors in standard multilevel interconnect silicon technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no.1, pp. 100–104, January 1996.

[102] C. P Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for si-based RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May 1998.

[103] J. Y. Chang, A. Abidi and M. Gaitan, "Large suspended inductors on silicon and their use in 0.2 μm CMOS RF amplifier," *IEEE Electron Device Letters*, vol. 14, no. 5, pp. 246–248, May 1993.

[104] M. Steyaert, A. van Roermund, and J. H. Huijsing, *Analog Circuit Design*. Kluwer Academic Publishers, 2006.

[105] J. Van der Tang, D. Kasperkovitz, and A. Van Roermund, *High-Frequency Oscillator Design for Integrated Transceivers*. Kluwer Academic Publishers, 2003.

[106] A. Natarajan, A. Komijani, A. Hajimiri, "A fully integrated 24-GHz phased-array transmitter in CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2502–2514, Dec. 2005.

[107] J. Crols, and M. Steyaert, "A fully integrated 900 MHz CMOS double quadrature downconverter," in *IEEE Int. Solid-State Circuits Conf. Digest*, 1995, pp. 136–137.

[108] J. Fenk W. Birth, R. G. Irvine, P. Sehrig and K. Schon, "An RF front-end for digital mobile radio," in *Proc. Bipolar Circuits and Technology Meeting*, 1990, pp. 244–247.

[109] F. Behbahani F. A. Fotowat-Ahmady, S. Navid, R. Gaethke and M. Delurio, "An adjustable bipolar quadrature LO generator with an improved divide-by-2 stage," in *Proc. Bipolar Circuits and Technology Meeting*, 1996, pp. 157–160.

[110] M. Elsayed, and M. I. Elmasry, "Low-phase-noise LC quadrature VCO using coupled tank resonators in a ring structure," *IEEE J. Solid-State Circuits*, vol. 36, pp. 701–705, April 2001.

[111] P. Vancorenland, and M. S. J. Steyaert, "A 1.57 GHz fully integrated very low-phase-noise quadrature VCO," *IEEE J. Solid-State Circuits*, vol. 37, pp. 653–656, May 2002.

[112] M. Tiebout, "Low-power low-phase noise differentially tuned quadrature VCO design in standard CMOS," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1018–1024, July 2001.

[113] A. Roufougaran, J. Rael, M. Rofougaran, and A. Abidi, "A 900 MHz CMOS LC-oscillator with quadrature outputs," in *IEEE Int. Solid State Circuits Conf. Digest*, 1996, pp. 392–393.

[114] L. B. Oliveira, J. Fernandes, I. M. Filanovsky, and C. J. M. Verhoeven, "A 2.4 GHz CMOS quadrature LC oscillator-mixer," in *Proc. IEEE Int. Symp. Circuits and Systems,* 2004, pp. 165–168.

[115] P. Andreani, "A low-phase-noise quadrature low-phase error 1.8 GHz quadrature CMOS VCO," in *IEEE Int. Solid State Circuits Conf. Digest,* pp. 290–291.

[116] J. Van der Tang, P. van de Ven, D. Kasperkovsky, and A. van Roermund, "Analysis and design of an optimally coupled 5-GHz quadrature LC oscillator," *IEEE J. Solid-State Circuits,* vol. 37, pp. 657–661, May 2002.

[117] C. Verhoven, J. Long, and I. M. Filanovsky, "Synchronization of Two LC-Oscillators Using Nonlinear Models," Private communication.

[118] L. B. Oliveira, A. Allam, I. M. Filanovsky, and J. R. Fernandes, "On phase noise in quadrature cross-coupled oscillators," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2005, pp. 2635–2638.

[119] H. C. Chang, X. Cao, U. K. Mishra, and R. York, "Phase noise in coupled oscillators: theory and experiment," *IEEE Transactions on Microwave Theory and Technique*, vol. 45, no. 5, pp. 604–615, May 1997.

[120] I. M. Filanovsky, A. Allam, L. B. Oliveira, and G. R. Fernandes, "Synchronization of van der Pol oscillator by external voltage of doubled frequency," in *Proc. IEEE Int. Midwest Symposium on Circuits and Systems,* vol. 1, 2006, pp. 56–59.

[121] K. F. Theodorchik, *Auto-oscillating Systems*. (in Russian), Technical Literature Pub. House, Moscow, 1952.

[122] D. A. Linkens, "Stability of the entrainment conditions for a particular form of mutually coupled van der Pol oscillators," *IEEE Transactions on Circuits and Systems, vol. CAS-23*, no. 2, pp. 113–121, February 1976.

[123] S. Gierkink, S. Levantino, R.C. Frye, C. Samori, and V. Boccuzzi, "A low-phase-noise 5 GHz CMOS quadrature VCO using superharmonic coupling," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1148–1154, July 2003.

[124] P. Tortori, D. Guerminandi, E. Franchi, and A. Gnudi, "Quadrature VCO based on second harmonic locking," in *Proc. IEEE Int. Symp. Circuits and Systems,* vol. 1, 2004, pp. 169–172.

[125] I. M. Filanovsky, A. Allam, L. B. Oliveira, and G. R. Fernandes, "Quadrature van der Pol oscillators using second harmonic coupling," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2006, pp. 1663–1666.

[126] A. Allam, I. M. Filanovsky, L. B. Oliveira, and J. R. Fernandes, "Synchronization of mutually coupled LC-oscillators," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2006, pp. 4297–4300.

[127] L. Romano, S. Levantino, C. Samori, and A. L. Lacaita, "Multiphase LC oscillators," *IEEE Transactions on Circuits and System-I, Regular Papers*, vol. 53, no. 7, pp. 1579–1588, July 2006.

[128] L. B. Oliveira, I. M. Filanovsky, and C. J. M. Verhoeven, "Exact calculations of amplitudes and frequency in a RC-Oscillator with quadrature outputs," *IEEE Int. Midwest Symp. Circuits and Systems*, vol. 1, 2004, pp. 413–416.

[129] J. Fernandes, M. Kouwenhoven, and C. van den Bos, "The effect of mismatch and disturbances on the quadrature relation of a cross-coupled relaxation oscillator," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 1, 2001, pp. 476–479.

[130] L. B. Oliveira, J. Fernandes, M. Kouwenhoven, C. van den Bos, and C. J. M. Verhoeven, "A quadrature relaxation oscillator-mixer in CMOS," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 1, 2003, pp. 689–692.

[131] C. J. M. Verhoeven, "First Order Oscillators," Ph.D. thesis, Delft University of Technology, Delft, The Netherlands, 1990.

[132] S. Gierkink, "Control Linearity and Jitter of Relaxation Oscillators," Ph.D. thesis, University of Twente, The Netherlands, 1999.

[133] H. Morimura, S. Shigematsu, and K. Matchida, "A Novel sensor cell architecture and sensing circuit scheme for capacitive fingerprint sensors," *IEEE J. Solid-State Circuits*, vol. 35, pp. 724–731, May 2000.

[134] A. Allam, and I. M. Filanovsky, "High frequency channel noise measurement and characterization in deep submicron MOSFETs," in *Proc. IEEE Int. Midwest Symposium on Circuits and Systems*, 2007, pp. 1348–1351.

[135] A. Allam, and I. M. Filanovsky, "Experimental comparison of coupling effects on the performance of quadrature CMOS LC and RC oscillators," in *Proc. Midwest Symposium on Circuits and Systems*, 2007, pp. 606–609.

[136] I. M. Filanovsky, M. M. Reja, and A. Allam, "A new configuration of CMOS two-stage wide-band amplifier," in *Proc. IEEE Int. Midwest Symposium on Circuits and Systems*, vol. 3, 2004, pp. 13–16.

[137] M. M. Reja, A. Allam, and I. M. Filanovsky, "A new CMOS wideband RF front-end for multistandard low-IF wireless receivers," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 3, 2005, pp. 2120–2123.

[138] I. M. Filanovsky, F. Fang, A. Allam, and K. Iniewski, "0.6 V supply voltage references for CMOS technology based on threshold-voltage difference architecture," in *Proc. IEEE Int. Midwest Symposium on Circuits and Systems*, vol. 2, 2005, pp. 1790–1793.

[139] I. M. Filanovsky, V. Ivanov, F. Fang, and A. Allam, "Sub 1-V supply CMOS voltage reference based on asymmetric differential stage with feedback," in *Proc. IEEE Int. Midwest Symposium on Circuits and Systems*, vol. 1, 2006, pp. 127–130.

[140] Y. Wu, "A low phase-noise LC voltage controlled oscillator," M. Eng. report, University of Alberta, December 2002.